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Japan:
Equipment To Tackle 256M DRAMs

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Equipment To Tackle 256M DRAMs

Exposure Equipment Usable With 256M DRAMs

936C1099A Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 68-71

[Article by Hiroaki Morimoto, LSI Laboratory, Mitsubishi Electric Corp.]

[Text]

Introduction

Although the present photoexposure technology used in LSI manufacturing seems to be approaching its limits in terms of both resolution and depth of focus, attempts are being made to use DUV (deep UV) to fabricate the 0.2 to 0.25 μm patterns required for the fabrication of 256M DRAMs.

Figure 1 [photo not reproduced] shows the 0.24 μm L&S pattern fabricated with a KrF excimer laser stepper using a Levenson-type phase-shifting mask. The stepper has an NA of 0.42 and the resist is SNR-248 manufactured by Shipley. Figure 2 shows the depths of focus (DOF) obtained at NAs from 0.4 to 0.6 with I-ray and KrF excimer laser-light sources. Here, the DOF refers to the defocusing amount providing the optical image of an L&S pattern with a contrast of 60 percent or more. This figure shows that, by adopting auxiliary means such as phase shifting,[1,2] various shapes of illumination,[3,4] and spatial filters[5] and exploiting new technology, the required degree of DOF can be obtained from 0.3 μm patterns with I-rays and 0.2 μm patterns with DUV. Consequently, there is a strong possibility that present photoexposure technology, with some improvements, can be used up to 256M DRAMs.

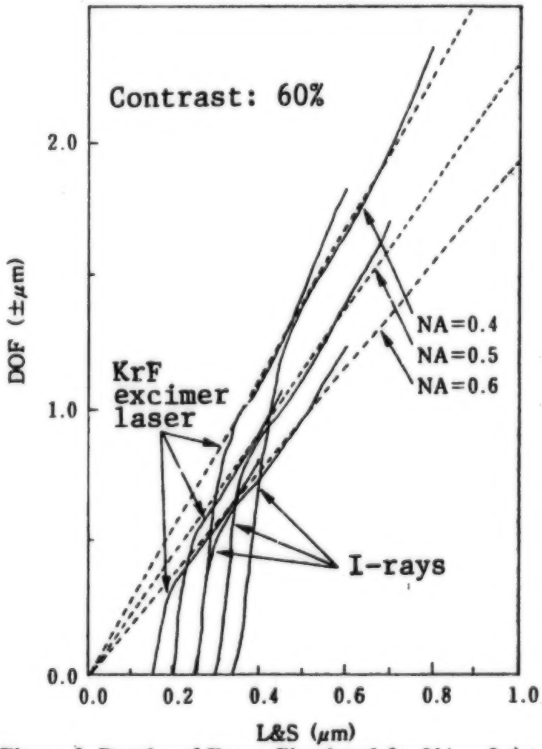

Figure 2. Depths of Focus Simulated for NA = 0.4 to 0.6 With I-Ray and KrF Excimer Laser-Light Sources

Even when the use of DUV may make manufacturing of 256M DRAMs possible in terms of resolution, it is expected that there will still be a limitation in terms of DOF margin and alignment accuracy. Also, further improvements in materials, processes, and cost are required to allow the use of DUV lithography in mass production.

The discussion in this report centers around these points.

DOF Margin

As seen in Figure 2, DOF tends to decrease as the pattern gets finer. Nevertheless, a certain DOF margin is required to use the technology in mass production. Table 1 shows examples of the required DOF obtained on the basis of various factors[6,7] and the targets to be achieved in the near future. If a 0.2 μm rule pattern is to be fabricated with a KrF excimer laser stepper, a decrease in the DOF is inevitable even when auxiliary means such as phase shifting is used, so it is necessary to reduce the DOF requirement to as low as possible. Factors involving DOF requirements include those associated with the wafer and those associated with the stepper, and the most important factor lies in device height differences on the wafer. While efforts have recently been made to reduce height differences, these are limited by device structures and cost. Wafer flatness has been improved in spite of increased diameter, but further improvements of the LTV is still desirable. Most of the factors associated with the stepper are related to image plane errors and the detection and reproduction accuracy of auto focusing. To deal with this, a method using multipoint focusing has been introduced to allow setting optimum focusing according to each device.[8] It is also desirable to improve the focusing detection and setting accuracy itself. The required DOF is the sum of these factors; presently about 2 μm. If the target values can be achieved, the necessary DOF may be decreased to 1.2 μm.

Table 1. Details of Required DOF

Item		Present	Target
Factors associated with wafer	Maximum height difference on wafer	0.6 μm	0.4 μm
	LTV of wafer	0.5 μm	0.3 μm
Factors associated with stepper	Curvature or inclination of image plane of optical system	0.5 μm	0.2 μm
	Auto focusing detection and reproduction accuracy	0.3 μm	0.2 μm
Total = Required DOF		1.8 μm	1.2 μm

Alignment Accuracy

Alignment accuracy has a value of 30 percent to 40 percent of the minimum pattern width. If alignment accuracy does not improve as resolution improves, integration would be limited due to the necessity of alignment margin. Table 2 shows the present alignment accuracy and the target alignment accuracy for 256M DRAMs of each factor.[6,9] If the minimum pattern size of a 256M DRAM is 0.2 to 0.25 μm, the required alignment accuracy is around 0.08 μm.

Table 2. Details of Alignment Errors

Item		Present	Target
Factor associated with wafer	Distortion of substrate wafer	0.05 μm	0.02 μm
Factor associated with mask	Mask pattern position error	0.15 μm/5 = 0.03 μm	0.10 μm/5 = 0.02 μm
Factors associated with stepper	Lens distortion	0.08 μm	0.05 μm
	Alignment error	0.08 μm	0.05 μm
	Magnification ratio error	0.03 μm	0.01 μm
Total (RMS)		0.13 μm	0.08 μm

In the course of fabrication, the wafer is subject to nonlinear distortion, which results in alignment errors. An alignment technique which corrects high-order nonlinear distortion by optimizing the sampling shot and the weight of each mark[3] is one approach aimed at reducing this error. Mask pattern position errors are mainly caused by the method by which the mask is held during electron-beam etching, temperature changes, beam drift, deflection distortion and stage-moving errors. The error is reduced to one-fifth on the wafer, but this is still significant.

Lens distortion is a factor very difficult to reduce, but it cannot be ignored in stepper matching. As well as minimizing the distortion, it is desirable to provide a function to correct distortion up to a high order for each stepper. Various new methods have been developed to reduce alignment errors and further improvements are forthcoming to improve stage accuracy.

A recently released step-and-scan system aligner[10] detects and corrects alignment and focusing during scanning to improve accuracy. Because the factors determining alignment accuracy will be more obvious as the accuracy improves, it is expected that in the future it will be even more difficult to improve accuracy, and it will be necessary to approach the problem simultaneously from the device side, such as the use of a self-alignment structure.

Cost of DUV Lithography

Figure 3 compares the calculated cost per layer of a single 8-inch wafer with I-ray and KrF excimer laser lithographies, assuming that the cost of I-ray lithography is 1. Costs related to equipment include the equipment price (depreciation of the stepper, coater and developer), throughput, operating ratio, maintenance cost, consumables and equipment area (clean-room costs). The percentage of mask cost varies depending on the types and number of input wafers. Resist cost includes the prices of resists and developing solutions. As can be seen in the figure, present excimer laser lithography is very expensive.

Causes of the increased costs of excimer laser lithography are the stepper price, consumables, maintenance cost and installation area of excimer laser equipment. In the future, it is expected that excimer laser equipment cost will compete with I-ray steppers by reducing the equipment price through mass production and by increasing the service life and frequency band of the excimer laser.

Few excimer-laser resists are available on the market, their prices are high at the present, and a large price reduction by mass production is essential in the future.

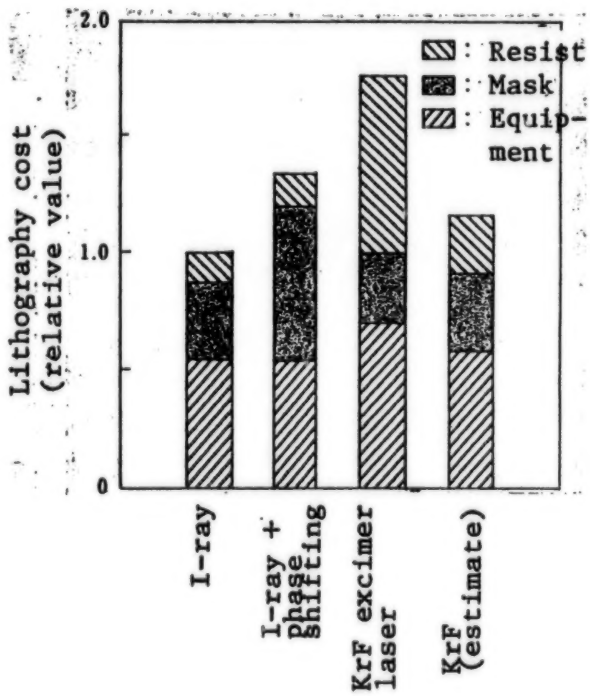

Figure 3. Example of Calculations of Cost per Layer of Single 8-inch Wafer

Mass production of excimer-laser resists may make it possible to reduce the cost below that of I-ray lithography, which uses phase-shifting techniques.

Lithography Technologies After 0.2 μm

Candidates being studied as lithography technologies after 0.2 μm include the use of ArF excimer laser light with a short wavelength of 193 nm, the use of VUV (Vacuum Ultra Violet) light emitted from an SR (Synchrotron Radiation) light source, the use of soft X-rays, and the electron beam drawing method. However, the use of short-wavelength light sources raises the problem of light absorption by optical components and resist; the use of X-rays is accompanied by the problem of mask fabrication accuracy due to its equal-magnification transfer; and the use of electron beam drawing is accompanied by problems in throughput and drawing accuracy. It is left for future research to identify if the

lithography after the 0.2 μm rule can be an extension of the present photoexposure system, or whether a change to another technique is necessary.

Conclusion

The 0.2 to 0.25 μm rule lithography required for 256M DRAMs may be dealt with by improving present photoexposure technology, but further improvements in equipment and devices are required in areas such as depth of focus and alignment accuracy. With regard to costs, price reduction is required through the mass production of equipment, maintenance, and materials. Although not mentioned in the above, improvements in processes such as the implementation of simple ARC (anti-reflection coating) are also important. It is desirable that these problems be surmounted by closer cooperation among the equipment, material, and device manufacturers.

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Etching Equipment Usable With 256M DRAM

936C1099B Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 72-75

[Article by Seiji Samukawa, Microelectronics Research Laboratories, NEC Corp.]

[Text]

Introduction

As we enter the age of 0.25 μm or below, more accurate etching technology is required. However, this technology is still in large part dependent on empirical factors, hence a scientific approach is difficult. This is because the plasma states and surface reactions are extremely complicated and there are not many means to analyze them. Even though our understanding is insufficient, plasma can be generated relatively easily and a very active state can be produced. However, various equipment using different methods has been introduced, adding to the confusion. Nevertheless, it seems the appropriate time to start discussions and studies for the ultrafine fabrication of 0.25 μm and below.

This report reviews the items required for etching equipment for 256M DRAMs and beyond.

High-Density Plasma Source

Most active discussions about etching equipment are related to the plasma source. Previously, a low-pressure, high-density plasma source always referred to ECR plasma. Now, a variety of plasma sources, including helicon-wave and inductive-discharge (Figures 1 and 2) have been developed and introduced in the market. Helicon-wave plasma and inductive-discharge plasma use the RF frequency band at around 10 MHz and do not require a ferromagnetic field, so they can be implemented with compact size and simplified design. On the other hand, they have problems controlling the discharge state due to insufficient understanding of the mechanism of plasma generation. It has also been pointed out that their large-surface electric fields and plasma potentials sputter or etch the walls, influencing the etching characteristic of substrates. On the other hand, with ECR plasma, progress has been made in the analysis of the plasma state and elucidation of the discharge mechanism, and optimization of the plasma state is very advanced. However, the use of microwave and ferromagnetic fields makes the equipment large and complicated. Another problem is the production of abnormal etched shapes on the gate electrodes, as shown in Figure 3, which occurs when electric charge is accumulated on the wafer because the capture rates of electrons and ions with respect to the field are different, such as in the case of the presence of a ferromagnetic field on the wafer.[1] Therefore, with ECR plasma, reduction of the magnetic field on the wafer electrode and size reduction are important topics to be considered.

As seen above, each plasma source has its merits and demerits. Nevertheless, when the equipment for manufacturing 256M and later DRAMs is considered, the trends of increasing the number of chambers and clustering are necessary, together with increasing wafer size. Further, a compact, simplified plasma source is necessary on actual mass-production lines. This means that size reduction is a

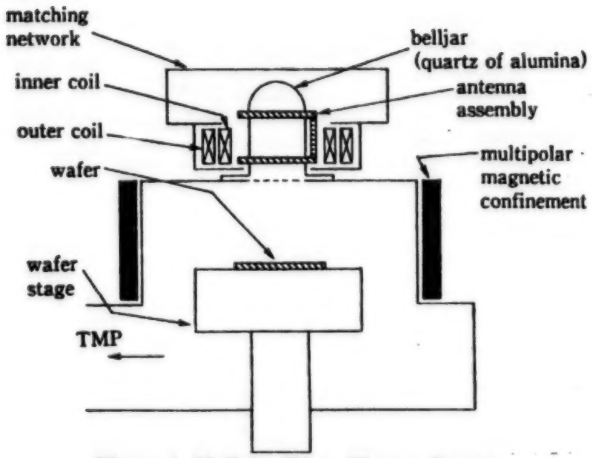

Figure 1. Helicon-Wave Plasma Source (mfd. Plasma & Materials Technologies)

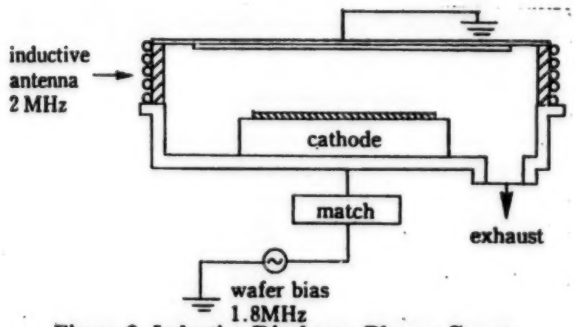

Figure 2. Inductive Discharge Plasma Source (mfd. by Applied Materials)

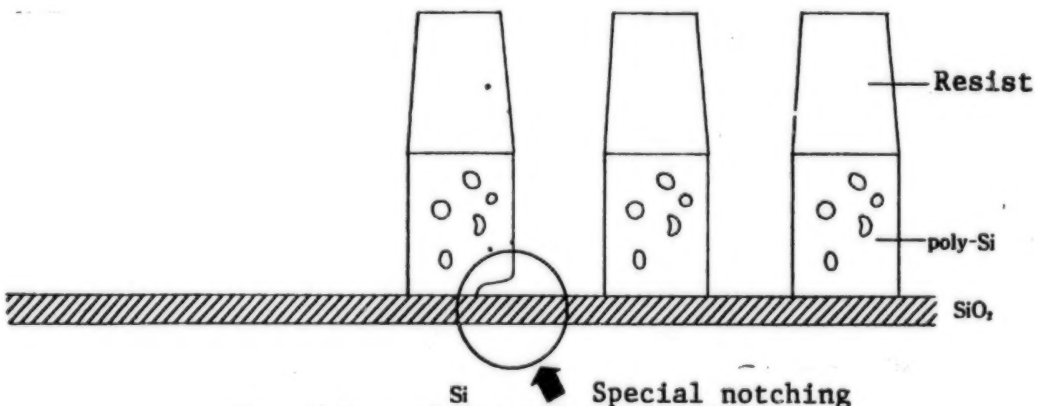

Figure 3. Abnormally Etched Shapes in Poly-Si Etching

necessary condition for ECR plasma sources to survive. This topic should be studied along with the decrease of applied frequency.[2] On the other hand, with helicon-wave plasmas and inductive-discharge plasmas, the optimization of plasma and optimization of hardware would be important issues in the future.

As described above, a variety of plasma sources have been developed and currently low-pressure, high-density plasmas have become the leaders in the etching process. However, it is becoming clear that high-density plasma is not always beneficial, as some problems have emerged due to the high density. Not all the active species in plasma contribute to the etching reaction; some of them produce the main reaction and others inhibit it. For example, polymerization in the etching of oxide film is determined by the ratio between the CF_2 radicals and F atoms in fluorocarbon plasma. The CF_2 radicals are the precursor of polymerization and F atoms function to inhibit polymerization. Therefore, to achieve highly selective oxide-film etching, the F/CF_2 radical-density ratio in the plasma should be low. However, in low-pressure, high-density plasmas, such as ECR plasma, helicon-wave plasma and inductive-discharge plasma, high electron temperatures and the occurrence of highly dissociative reactions tend to make polymerization inadequate due to a low CF_2 radical density. This poses problems such as a low etching selectivity with respect to silicon wafers.[3] To solve these problems while maintaining the benefits of low-pressure, high-density plasma, it is important to control the electron temperature and dissociative reaction in plasma. Controlling the generation of active species by pulse-modulated plasma was recently proposed as a method to solve these problems.[4]

In manufacturing 256M and later DRAMs, it is desirable that these problems be solved at the plasma source. Regardless, the mixed presence of a variety of plasma sources is not favorable for users, because this situation will require much effort in equipment selection and process development. A valuable future topic would be to identify the optimum plasma state for each type of material and develop a standardized plasma source that can achieve that state.

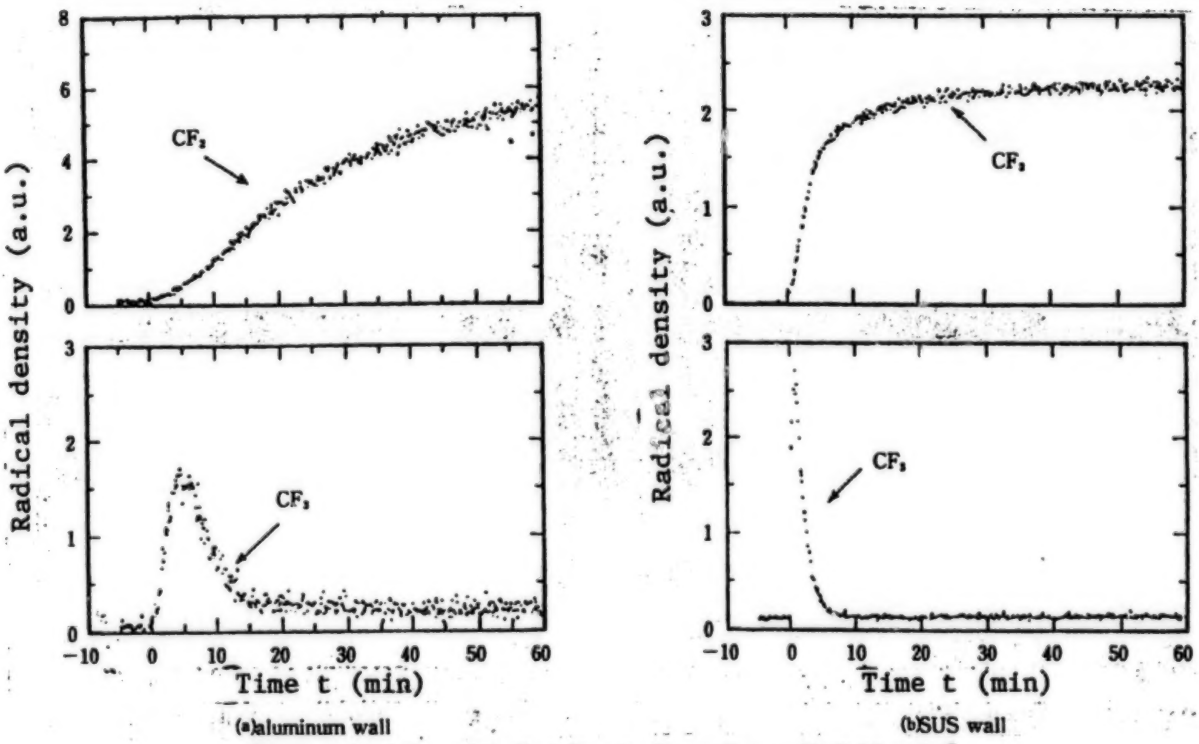

Figure 4. Variation of Radical Density Depending on Wall Material[5]

Role of the Chamber Wall

Although chamber wall material and chamber size are very important factors relating to plasma, they have not been studied sufficiently. Wall material and wall potential states (grounding, floating) have a great effect on the plasma's potential distribution and charged particle decay times. As they vary, the electron loss probability on the wall surface, the electron temperature in plasma, plasma potential, and floating potential are also varied so the ion impact state onto the wall is also varied. In addition, as the reactivities of active species (radicals, ions) are variable depending on the wall materials, as shown in Figure 4, their loss and adsorption probabilities are also varied which varies the percentage of active species existing in the plasma.[5] This is why it is said that the reproducibility of plasma processes is largely affected by the wall. Therefore, the selection of wall material and its electric state are also important themes for equipment implementation.

Chamber size is also important. Chamber size increases when the size of the wafer is increased, and the increase in chamber size means a relative increase in the volume of plasma with respect to the wall, providing the benefits of reduced electron loss and lower plasma potential and electron temperature. Therefore, the optimization of chamber size is also an important topic to be considered.

Exhaust System

The exhaust system is noteworthy from the viewpoint of controlling the residence time of reaction products as well as controlling the degree of etching vacuum. Since the gas flow varies the residence time of reaction products and thereby the etching characteristic as shown in Figure 5.[6] Exhaust system design is an important element in the design of etching equipment. Equipment design must take conductance into full consideration, as well as the exhaust rate of the turbo-molecular pump.

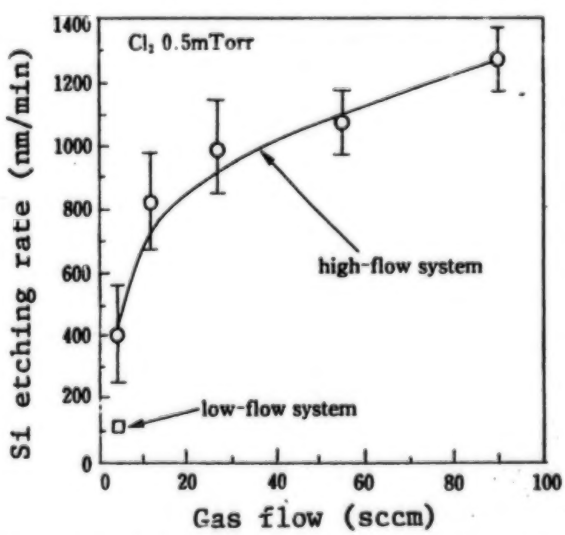

Figure 5. Variation of Etching Characteristic Depending on Gas Flow

Multi-Chamber Equipment

Microfabrication and the multi-layer structure of devices are making the etching process increasingly complicated. As a result, it has sometimes become necessary to apply pre- and post-processing to etching, use processes for etching layered film with several gas systems, or process several large-size wafers simultaneously. An increase in the number of chambers is indispensable to achieve these. In addition, as continuous processing in vacuum is essential to process reproducibility, the implementation of equipment as standardized cluster tools is also necessary. This is an important subject which could lead to the standardization of etching equipment.

Conclusion

In the above I reviewed the points concerning etching equipment expected for use for 256M DRAMs and later. The extremely stringent accuracy requirements for etching have made it necessary to conduct an advanced study of the equipment. This requires an approach to the plasma process aimed at achieving optimum cost efficiency and expected characteristics. Equipment standardization has also become an important topic. These requirements are extremely severe for equipment manufacturers, and I hope our research will contribute to their efforts.

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Ashing Equipment Usable With 256M DRAMs

936C1099C Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 76-79

[Article by Toshiyuki Orita, Process Technology Center, Oki Electric Industry Co., Ltd.]

[Text]

Introduction

Resist removal at the final stage of a lithography process is one of the best-known processes in LSI manufacturing. Resist is usually removed by dry/wet processes. The technology for dry removal of resist using oxygen plasma (hereinafter referred to as ashing) has been used widely for more than a decade. Problems in the ashing process include damage such as charge-up and metal contamination, and the ashing residue. This report describes ashing technologies usable with 256M DRAMs.

Damage

Damage produced in the ashing process can be divided into four categories: metal contamination, charge-up, ion impact damage, and UV irradiation damage. Each of these will be described below.

1. Metal Contamination

When an alkali metal (usually Na) is implanted in SiO_2 during ashing, mobile ions are generated varying the threshold voltage of MOS transistors. Similarly, the implantation of heavy metal in an Si wafer or Si_2 causes stacking faults, or a deterioration of the withstand voltage of the gate-oxide film of MOS transistors. It is agreed that the target value of metal contamination with 256M DRAMs should be no more than $1 \times 10^9/cm^2$.

With ashing using oxygen plasma, the metal oxides in the resist cannot be removed due to the low vapor pressure, and hence remain on the wafer surface. There are even cases in which the metal penetrates the oxide film, depending on the processing condition of the ashing. The major causes of this are ion impact (knock-on), charge-up, and temperature, but the detailed mechanism is not yet known.

Success in the reduction of metal contamination lies in reducing the influence of charged particles, so the use of down-flow ashing or ozone ashing is optimum for this purpose. From the viewpoint of the process, studying the addition of H_2O,[1] or low-temperature ashing may be necessary.

2. Charge-Up

In the ashing process, charged particles in the plasma cause charge-up and degrade the withstand voltage of the gate insulation film. This charge-up can be evaluated by measuring the V_{fb} shift of MNOS diodes. With this method, after previously identifying the relationship between the voltage applied to the gate of MNOS diodes, V_a, and the V_{fb} shift (ΔV_{fb}), the relative potential and polarity of the gate electrode with respect to the Si wafer is estimated from ΔV_{fb} after plasma processing. Figure 1 shows the structure of an MNOS diode, and Figure 2 shows the relationship between the voltage applied to the gate of an MNOS diode, V_a, and the V_{fb} shift (ΔV_{fb}) when the voltage application period is 1 minute. The detection limit in ΔV_{fb} evaluation is variable depending on the sample structure and measuring method, but in general it is +/- 0.1 V with ΔV_{fb}. Among the currently available ashing equipment, the equipment with ΔV_{fb} within +/- 0.1 V uses the down-flow system as with coaxial ashing equipment (with the electrode design optimized) and microwave down-flow ashing equipment (with the chamber structure optimized) or does not use plasma as with ozone ashing equipment. The equipment providing smaller ΔV_{fb}, while performing ashing processing in plasma, includes the helical asher ($\Delta V_{fb} \leqq$ +/- 0.25 V) and microwave asher ($\Delta V_{fb} \leqq 0.4$ V).

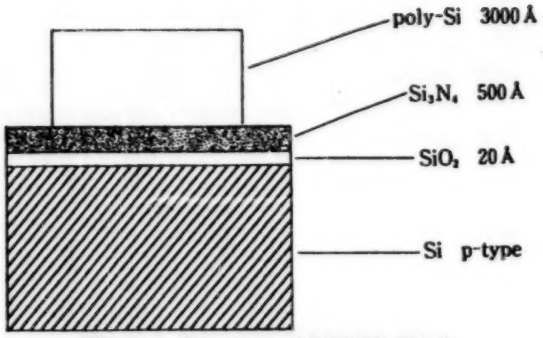

Figure 1. Structure of MNOS Diode

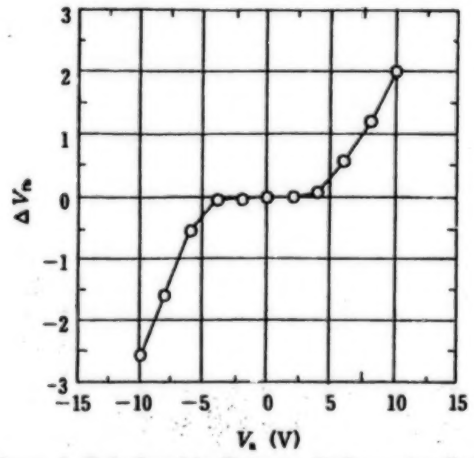

Figure 2. Relationship Between Voltage Applied to MNOS Diode Gate, V_a, and V_{fb} Shift, ΔV_{fb}

charge-up by applying the down-flow system in which the wafer is separated from the plasma discharge area, or by improving the uniformity of plasma density through the optimization of the equipment or process.

3. Ion Impact Damage

Ion impacts cause the knock-on of metals, sputtering and crystal defects. Ion impact energy is determined by the difference between the plasma potential and wafer potential. Crystal defects can be evaluated by thermal wave measurement. Figure 3 shows the results of thermal wave measurements by irradiating four kinds of plasma. The down-flow (coaxial) ashing equipment presents an identical thermal wave signal level to the reference; the microwave ashing equipment, which exposes the wafer to plasma, increases the signal level slightly; and the O_2 RIE equipment (V_{DC} = -100 V), which uses a large ion impact energy, increases the signal level drastically.

4. UV Irradiation Damage

When vacuum UV rays (λ = 140 nm or less) above the band gap energy of SiO_2 (8.8 eV) is irradiated, electron-hole pairs are produced in SiO_2 and the holes are trapped near the interfaces.[3] It has also been reported that, in a photo-etching experiment, neutral traps were produced by etching using UV rays with λ = 194 nm.[4]

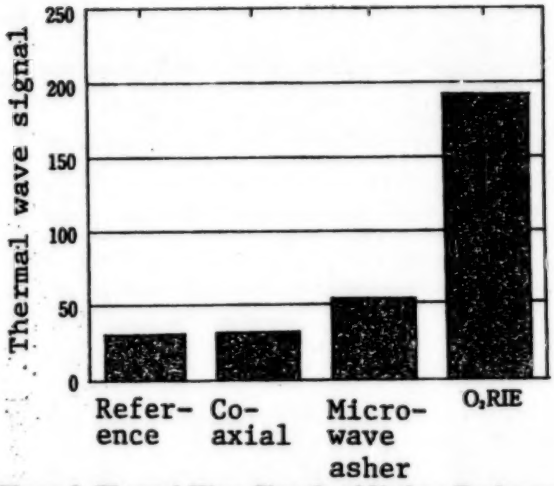

Figure 3. Thermal Wave Signals of Various Equipment

As seen from the above, it is desirable to avoid UV rays with λ = 200 nm or less as much as possible.

Problems in Resist Removal

As it is said that particles of more than one-fifth to one-tenth the minimum fabrication size degrade the device characteristics and decrease yield, the production of particles with diameters of more than 0.05 to 0.02 μm should be minimized with 256M DRAMs (0.25 to 0.20 μm process). There has been little research on the removal of these particles (residues) in ashing, but the basic orientation may be to use ashing for the removal of organic components (resist) and use a wet process for the removal of inorganic components (metals, etc.), contained in the resist. (It is desirable that ashing turns the inorganic components into a state easily removable by a wet process at the same time as removing the organic components.)

Resist removal by the ashing process is specially difficult in cases where the resist is hard to release due to modification after high-dose ion implantation, for example, and in cases where the reaction products attached during etching remain as residues after aluminum etching or gate etching. These examples will be described in detail below.

1. Resist Removal After High-Dose Ion Implantation

When high-dose ions are implanted using a positive resist as the mask, the rise in temperature due to ion impact degrades the resist surface, causing a drastic drop in the ashing rate in cases where the ashing is based on oxygen radicals. If ashing is processed at high temperature to increase the ashing rate, a phenomenon in which the resist splits into small pieces (pumping) occurs, and the resist turns into a state in which complete removal is impossible (a state in which oxidation is difficult).

Figure 4 [photos not reproduced] shows a cross-sectional SEM micrograph after the pumping of a resist. The pumping is considered to be due to the emission of N_2 or other degases from the lower part of the resist that has not been degraded by high-temperature ashing. The pumping can be prevented by eliminating the gases in

the resist by applying UV curing or hard baking to the resist before ion implantation. However, a fine residue is produced in the case of ashing based on oxygen radicals, even after UV curing or hard baking. For the present, such residue is removed by post-cleaning.

The most effective method to remove the degenerated layer on the surface is ashing using the reaction with ion impact. It has been reported that $H_2O + H_2$ RIE is capable of complete dry removal of ion-implanted resist.[5] However, as plasma processing, such as RIE, is accompanied by the potential of charge-up, ion impact damage, and contamination due to the chamber, such damage must be reduced.

2. Resist Release After Aluminum Etching

Figure 5 [photo not reproduced] shows a cross-sectional SEM micrograph of the result of ashing with O_2 plasma after aluminum etching. The residue shown in the photo is a compound of the aluminum sputtered during etching. A similar residue is also produced after via hole etching.

Figure 6 [photo not reproduced] shows a cross-sectional SEM micrograph after via hole etching. This residue has previously been removed by ashing and a chemical solution process, but it has recently been reported that it can be removed by $F + H_2O$ down-flow ashing and pure water processing.[6]

The proposed mechanism is to substitute the aluminum compound with fluoride by $F + H_2O$ down-flow ashing and dissolve it in pure water.

To deal with aluminum corrosion, a system has been implemented in which the etching equipment, ashing equipment, and wet tank are coupled to perform resist removal continuously in vacuum.

3. Resist Release After Gate Etching

Highly selective etching of poly-Si uses HBr gas. When poly-Si etched with an HBr-type gas is ashed with O_2 plasma, a residue is produced on the resist sidewalls.[7] This residue is silicon oxide film produced when $SiBr_x$ deposited during etching reacts in the atmosphere. A similar residue is also observed in low-temperature etching of poly-Si using Cl_2 gas.[8] This residue can be removed by wet etching (SiO_2) but removal through ashing is being studied to reduce the decrease of the film on the base SiO_2. There has been a report that it can be removed by $O_2 + CF_4$ down-flow ashing.

Conclusion

Ashing methods which do not damage devices of the 256M DRAM class may be low-temperature ashing of the down-flow or ozone-type which cuts UV rays of λ = 200 nm or less.

Reduction of fine residue (with diameters of 0.05 to 0.02 μm or more) is a concept left for the future.

Resist remaining after high-dose ion implantation can be removed either by the complete-removal method using plasma or by the method using ashing (down-flow or ozone system) based on oxygen radicals by combining post-processing such as UV curing and hard baking and post-cleaning. One of these methods may be selected depending on the reduction of fine residue and damage in the equipment using plasma.

There are cases in which reaction products deposited during etching tend to remain as residue after post-etching resist release. A method of adding fluorine-type gas has been proposed to remove the residue, but since the addition of such gas results in etching of Si and SiO_2, this requires an improved selection ratio (with respect to Si and SiO_2), an improved ashing rate, uniformity, and stable end-point detection. As the production of residue after post-etching resist release is in large part affected by the etching technology, new problems are expected to occur as etching technology changes in the future.

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Ion Implantation Equipment Usable With 256M DRAMs

936C1099D Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 80-83

[Article by Takashi Murakami, Taketo Takahashi, and Yoji Kawasaki, Second LSI Process Development Dept., Mitsubishi Electric Corp.]

[Text]

Introduction

Ion implantation equipment has advanced following the increased density of DRAMs, which are the leading devices fabricated using ultra-large-scale integration. Figure 1 shows the changes in the design rule, wafer size, and ion implantation technology used with each generation of DRAMs. In recent years, oblique rotation implantation equipment has been put to practical use

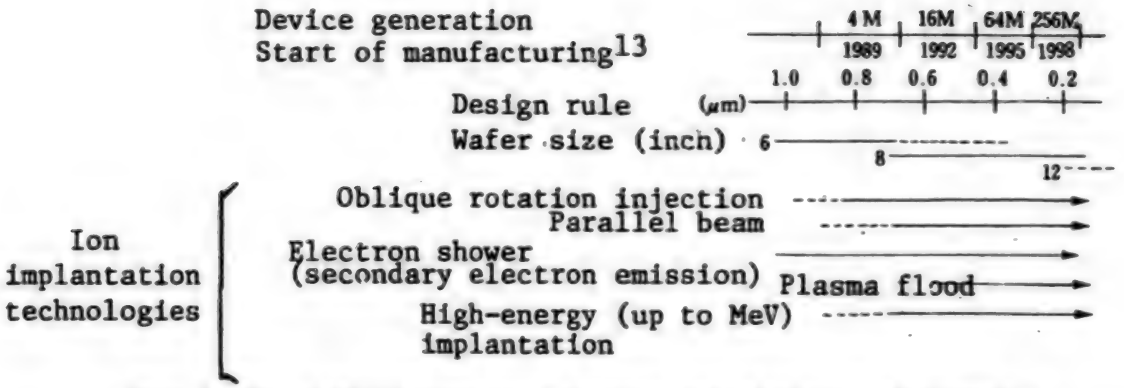


Figure 1. Different DRAM Generations and Changes in Ion Implantation Technologies

with medium-current machines, and parallel-beam equipment has also been developed. With large-current machines, the electron shower has been improved to reduce charge-up and a high-performance plasma flood gun has been developed. High-energy (up to MeV) ion implanters have passed the R&D stage and are now starting to be used in mass production. In addition to the above, 256M DRAMs with more advanced microminiaturization require the improvement of low-energy implantation performance for the fabrication of shallow junctions. Previous technological trends—that is the requirements to reduce the particles, contamination and charge-up, and improve implantation accuracy—will become more severe following the microminiaturization of devices and the increase in wafer size. On the other hand, in actual equipment operation, improvements in the basic performance of production facilities such as automation, higher operating ratios, and easy maintenance will also be important.

This report describes the requirements of these items from the user perspective for the ion implantation equipment to be used with 256M DRAMs.

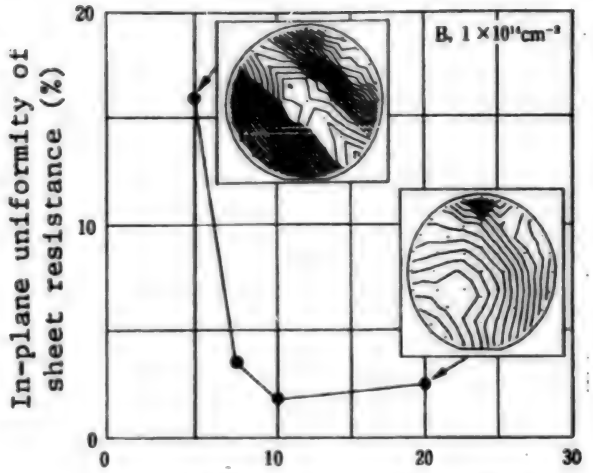
Low Energy Implantation

Technology for the fabrication of shallow junctions is important for 256M DRAMs with a junction depth of about 0.1 μm. Formation of junctions in the particularly shallow p^+ layer is difficult and has been dealt with by BF_2 implantation[1] or pre-amorphizing implantation.[2,3] The BF_2 implantation is advantageous with its possibilities of lowering the virtual acceleration energy and increasing the beam current. However, its use in processes is restricted due to such problems as the roughness of high-melting-point metal surfaces due to fluorine[4] or the segregation of fluorine, which was redistributed during annealing, in residual defects near the interface between the amorphous layer and single crystals.[5] Pre-amorphizing can be achieved by a method using Si or Ge[2] or a method using N[3] but in any case B[3] should be implanted at no more than 10 keV to obtain shallow junctions. However, if implantation energy is decreased using a conventional, electrostatic-scanning-type medium-current machine, the in-plane uniformity deteriorates as shown in Figure 2(a). This is thought to be because the in-beam charge density becomes non-uniform as the beam expands during beam travel. In addition, medium-current machines with parallel-beam implantation are also required to maintain beam parallelism at low energy. On the other hand, large-current machines also have problems in the decrease of beam current and drop of throughput when the implantation energy is decreased as shown in Figure 2(b). With large-current machines, it is desirable to develop equipment which allows uniform implantation and high throughput even at low energy.

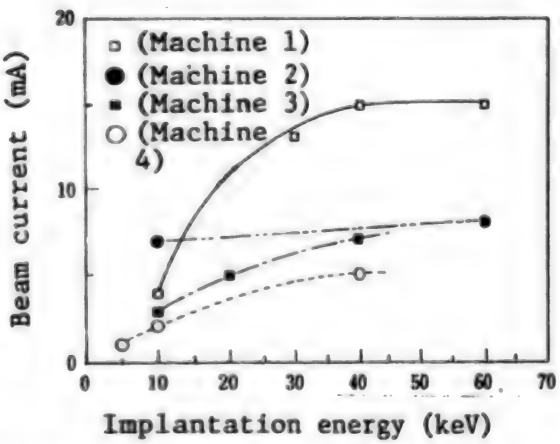
Charge-Up

Electrostatic breakdown due to charge-up is dependent on the device structure, manufacturing flow, and ion-implantation conditions. Increase in integration scale makes the gate-oxide film thinner and gate area smaller, and the increase in wafer size requires implantation with a larger beam current to assure the required throughput. These factors are intensifying the problem of electrostatic breakdown.

To reduce electrostatic breakdown, attempts have been made to reduce the charge density of the ion beam in ion implantation equipment by neutralizing charges with an electron shower and enlarging the ion beam diameter. The first electron showers developed irradiated the target with primary electrons and supplied the generated secondary electrons to the wafer. However, problems have been found with the re-entry of primary electrons with high energy, and in the response of the feedback control of the amount of irradiation. To deal with these problems, methods are being studied for preventing the arrival of high-energy electrons at the wafer by applying a magnetic or electric field[6,7] and a plasma-flood method which produces plasma near the wafer to prevent its charge-up with electrons. The plasma-flood method is attractive in principle because it allows neutralization using low-energy electrons alone, and can assure a wide process margin without complicated condition setting. Conversely, additional study is required on the influence of generating a plasma near the wafer. Figure 3 shows an example of reduction of electrostatic breakdown using a plasma flood gun,[8] which has provided favorable results.



(a) Implantation energy dependence of in-plane uniformity of sheet resistance with medium-current machines



(b) Implantation energy dependence of boron-beam current with large-current machines

Figure 2. Implantation Energy Dependence of Ion Implantation Equipment

Enlarging the beam diameter is also effective for reducing electrostatic breakdown, and equipment should be designed considering contamination due to sputtering in the beam line.

Particles and Contamination

About 80 to 90 percent of defects in DRAMs from 64M to 256M are due to particles on the wafer or its contamination by metals. It is also said that 95 percent of all particles at the 256M DRAM level may be derived from

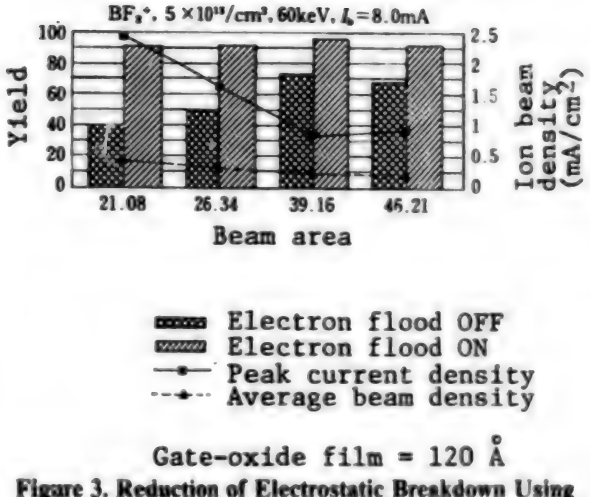


Figure 3. Reduction of Electrostatic Breakdown Using Plasma Flood (Electron Flood)[8]

the manufacturing equipment. Every equipment manufacturer has expended special efforts to ensure clean manufacturing, but as microminiaturization advances, particle control should involve smaller particle sizes and the equipment to meet this requirement. Figure 4 illustrates changes over time of the particles of specific implantation equipment. Particle control, considering particle diameters of 0.3 μm or more, may not identify any abnormality because it does not find a variation in the number of particles, but an increase in the number of particles due to an abnormality in a certain period can be identified by monitoring particles with diameters of 0.17 μm or more. As seen here, without due control and reduction by monitoring even very fine particles, the yield could drop while the cause would not be identified. The measurement of the number of particles gets difficult as the particle size decreases but, as it has been reported based on experience, even particles of around one-tenth the minimum size of the device can cause an adverse effect.[9]

It is well known that contamination by metals such as Fe, Cr, Ni, and Al in general increases the junction leakage

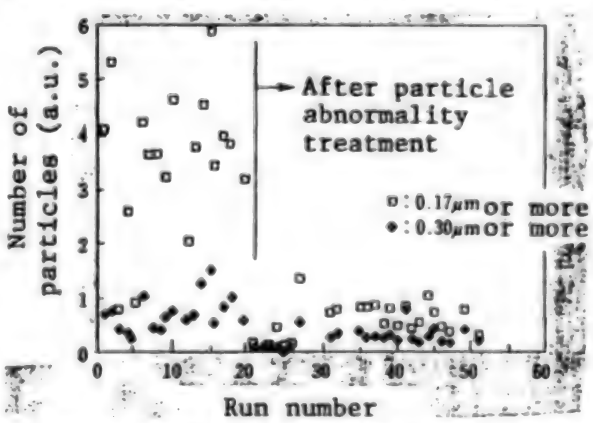


Figure 4. Changes in Number of Particles of Ion Implanters

current. The advancement of microminiaturization toward the 256M DRAM will increase the sensitivity to contamination due to shallower junctions and a smaller peripheral length reduction ratio.[10] This problem will increase if low-temperature annealing, which can reduce impurity diffusion, is used to form shallow junctions. Figure 5 shows an example in which metal contamination is reduced by covering with Si the part that would be sputtered by the ion beam. It achieved a low leakage current of 10^{-7} A/cm^2 even with low-temperature annealing at 500°C.[11]

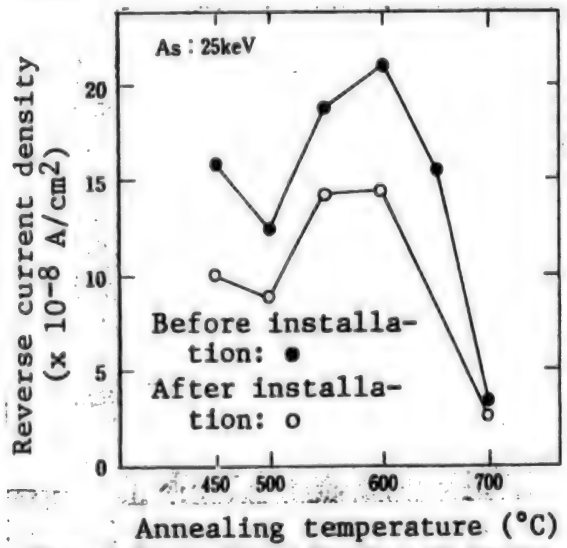


Figure 5. Reverse Current Density at n$^+$p Junction Depending on Annealing Temperature Changes

Compared to before installing the sputtering-prevention plate made of Si (filled circle), the characteristic after installation (o) is improved at any annealing temperature.[11]

Device microminiaturization will continue to drive the battle against particle and metal contamination.

Wafer Size Increase

Wafers with 8-inch or larger diameters will be used in the age of 256M DRAMs and it is highly probable that 12-inch wafers will be used in mass production.[12] To maintain the in-plane uniformities of the implantation quantity and depth even with large-size wafers, technology for aligning the ion beam incident angle in the wafer plane is essential for medium-current machines using ion-beam scanning. Reducing the in-plane variations in incident angle by using a longer beam line is advantageous in terms of its lower price but, when equipment size and performance are taken into consideration, the predominant equipment used in the future will be parallel-beam equipment.

Basic Performance of Production Facilities

Apart from the requirements for 256M DRAM-compatible ion implantation equipment from the viewpoint of process technology as described above, it is also important to improve the basic performance of ion implantation equipment by recognizing that it is a production facility.

To improve the operating ratio, what is required is to reduce the failure frequency and to extend the service life of the ion source. Reduction of the failure frequency may not need any explanation. Extension of the service life of the ion source has been attempted by extending filament life, but the implantation capability of recent equipment is often affected by discharges due to contamination inside the ion source as well as the filament life. Future improvements should take this into consideration.

While equipment automation has progressed, the error rate in the auto mode is so high that the reliability is not sufficient for use in automated fabrication in the age of the 256M DRAMs. This is not only due to software; errors also occur due to matching errors between software and hardware resulting from deviations in hardware adjustment. A reliable automated hardware/software system is necessary if the industry is to move forward.

As for the processing capacity, while the equipment is operating the processing capacity is determined by such factors as wafer transportation, beam set-up, implantation operation and beam shut-down. Of these, the operation which presently takes the most time is automatic beam set-up. This is especially true in the R&D line where continuous processing of several lots using the same implantation condition is rather rare, and much time is required for auto set-up every time the implantation condition is to be changed. Also, as the source condition varies gradually during use, there are cases in which the beam will not start smoothly with the initially set parameters. To allow quick auto-beam start-up regardless of source condition changes in time, a measure such as the provision of learning functions may be necessary. Obviously, there is much room for automation improvement.

It is almost needless to mention that for size reduction, operability and equipment safety are important. Recent equipment features better operability in the stationary state thanks to touch-screen input and various monitoring systems; operability and safety in non-stationary states such as during maintenance should also be considered. The equipment must be made user-friendly, for example, by designating the points where periodical maintenance is required to relieve operators of that concern.

Conclusion

We described above the performance required for 256M DRAM-compatible ion implantation equipment from the user standpoint. From the viewpoint of process technology, the important topic is to improve the low-energy implantation performance as well as the extensions of previous technological trends such as dust generation reduction, contamination reduction, charge-up reduction and implantation accuracy improvement. From the production viewpoint, the pursuit of improved reliability including reduced failure rate and ion source-life extension, automation, improved operability and greater safety is desirable.

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Oxidation, Diffusion and LP-CVD Equipment Usable With 256M DRAMs

936C1099E Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 84-88

[Article by Hirohito Watanabe and Koichi Ando, VLSI Device Development Research Laboratories, NEC Corp.]

[Text]

Introduction

The development of DRAMs, the leading vehicle of the semiconductor industry, has become more active, and 64M DRAMs have already been commercialized. Currently, active R&D is being conducted into 256M DRAMs featuring a higher scale of integration.

Manufacturing such ultra-large-scale integration silicon devices requires highly reliable manufacturing process technology with controlled surface, interface, and film quality. Oxidation, diffusion, and LP-CVD technologies are no exception and are being subjected to various requirements for improvement.

Figure 1 shows the design rule, junction depth, gate-oxide film thickness, and capacitance insulation film thickness of each generation of DRAM. The design rule values of 0.25 μm, junction depth of 0.075 μm, and gate insulation film thickness of 80 angstroms almost satisfy the actual trend. On the other hand, the thickness reduction of capacitance insulation film has been made less demanding by combining it with a three-dimensional electrode with increased electrode surface area. It is now possible to use silicon nitride capacitance film with a film thickness (when converted to oxide film thickness) of about 40 angstroms as the capacitance insulation film of 256M DRAMs, provided that the film has a good coating characteristic. On the other hand, highly dielectric film appears to be a promising technology for reducing the number of manufacturing processes, hence its development is presently being studied.

The necessary conditions for equipment used in manufacturing 256M DRAMs are: First, high-reliability technology compatible with the fabrication of ultra-large-scale integrated devices should be established and mass-producible equipment should be developed to implement them. Second, equipment compatible with an increased wafer size accompanying the increase in chip size and cost reduction should be developed. Nevertheless, if the wafer size increase leads to a rise in equipment cost or a drop in throughput, the purpose of equipment development itself would be lost. Third, the equipment cost and failure rate should be decreased by simplifying the equipment and promoting standardization. Presently, manufacturing equipment is getting more complicated by an increased number of components. This is the result of the implementation of accumulated equipment experience. But, in the future, it is necessary to promote the simplification of equipment by identifying the essence of each process and emphasizing only the

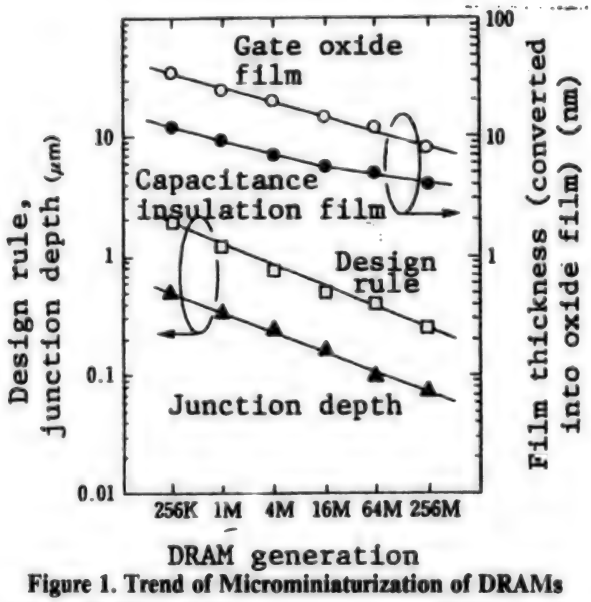


Figure 1. Trend of Microminiaturization of DRAMs

required functions. As well as reducing the number of components, it is also important to standardize equipment and components. By making such efforts it will be possible to reduce failure rate and the maintenance time even when the throughput is increased and clustering, which is effective in interface and surface control, is used.

There are many problems to be solved in the development of equipment as seen above, and this report discusses the required measures to solve them by enumerating some of the concepts and topics related to the technology for the fabrication of thin films and shallow junctions required to manufacture 256M DRAMs.

Annealing Equipment

Following the reduction of device size, the formation of shallow junctions and the reduction of the redistribution of impurities are required more urgently than before. Presently, impurities are mainly introduced by ion implantation. However, because activation processing and damage recovery after ion implantation require highly accurate control of temperature, time, and atmosphere, resistance-heating-type electric furnaces currently used are approaching their technical limits. This is because the individual wafers have different thermal hysteresis if they are transported in batches to the electric furnace, and reduction of thermal hysteresis is difficult.

RTP (rapid thermal processing) is utilized as the technology for compensating for this limitation of electric furnaces. RTP provides good throughput because it can activate impurities in a short period and it causes little diffusion of impurities as shown in Figure 2.[1] In addition, because of the advantages in its ability to handle wafers with increased size, this technology will be indispensable for manufacturing 256M DRAMs. However, its cold-wall design tends to radiate a great deal of heat from the wafer edges during heating, and uniformity in the wafer plane is difficult to achieve, sometimes causing crystal defects during heating. In addition, while the temperature is in general controlled by observing the infrared rays from the back of the wafer using a pyrometer, the infrared ray emission rate is often variable depending on the condition of the back of the wafer. Although RTP has already been put to practical use in some areas, there are many problems yet to be solved.

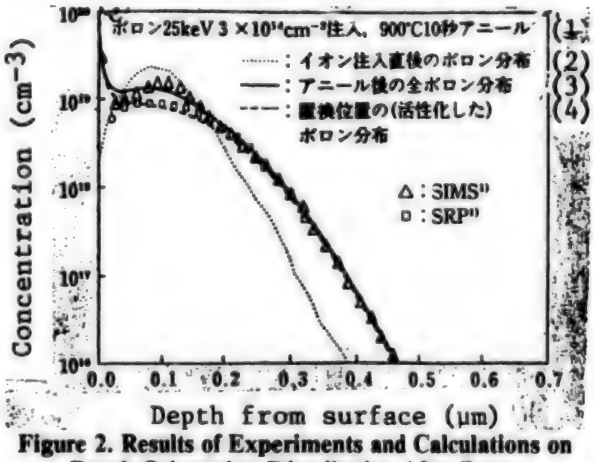


Figure 2. Results of Experiments and Calculations on Depth Orientation Distribution After Boron Implantation and Annealing

Key: 1. Boron 25 keV x 10^{14} cm^{-2} implantation, 900°C 10-second annealing; 2. Boron distribution immediately after ion implantation; 3. Total boron distribution after annealing; 4. (Activated) boron distribution of substituted position

RTP equipment has better properties than conventional electric furnaces as described above but, when considering throughput and other factors, the electric furnace is still superior in many processes and it is expected that the use of electric furnaces will continue in the fabrication of wells. The batch-type rapid thermal processing furnace which has been gathering interest[2] has the potential for providing the advantages of both RTP equipment and batch processing equipment and could be an effective method for fabricating 256M DRAMs in the future.

LP-CVD Equipment

Among the LP-CVD technologies to be used with 256M DRAMs, those which especially need improvements in the process equipment are the fabrication of ultrathin insulation film with excellent coating such as capacitance film, and the fabrication of silicon film used in wiring and electrode manufacture. The discussion that follows will focus on these technologies.

1. Capacitance Insulation Film Fabrication Equipment

Devices such as 256M DRAMs require thin film with a thickness of less than 40 angstroms, which is close to the physical limit, even if three-dimensional electrodes are combined as was described earlier. Control of natural-oxide film on the electrode surfaces is critical for the fabrication of such thin films.

Natural-oxide film is formed in the cleaning process, during exposure to the atmosphere between processes, and when the wafer is put into the nitride film deposition furnace. Active attempts have been made to reduce natural-oxide film growth during the furnace input operation through improvements in the equipment and pre-processing methods.

Development of LP-CVD equipment with a load-lock mechanism has also been undertaken to prevent atmospheric penetration during the furnace input operation.[3] This method replaces the wafer atmosphere in the leak-tight load-lock chamber with a high vacuum or high-purity inert gas atmosphere before transporting the wafer into the furnace.

From the viewpoint of process improvement, a method for reducing the natural-oxide film growth by applying RTN (rapid thermal nitridation) before input to the LP-CVD furnace has also been reported.[4]

These measures have been very effective in reducing natural-oxide film growth in the furnace, but could not remove natural-oxide film completely. Complete removal requires an in-situ oxide film-removal process and atmospheric-control technology with the oxygen partial pressure reduced below 10^{-6} Torr.

To make this possible, equipment is being developed which provides high-vacuum modules and combines several process modules called cluster tools. Also under development is equipment performing several processes in a single-process module.

With the general structure used by cluster tools, the natural-oxide film is removed in the pre-processing module installed inside the equipment and the wafers are transported into the film-fabrication module in a controlled atmosphere for deposition of the designed film. It has been reported that batch-type clustered equipment using fluoride vapor etching for post-processing can fabricate high-quality capacitance film with a thickness of around 40 angstroms.[5]

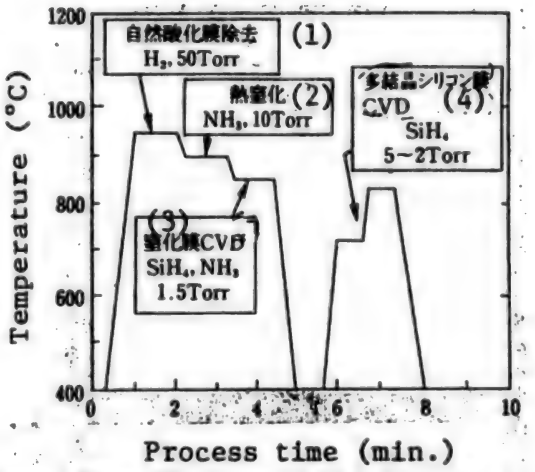
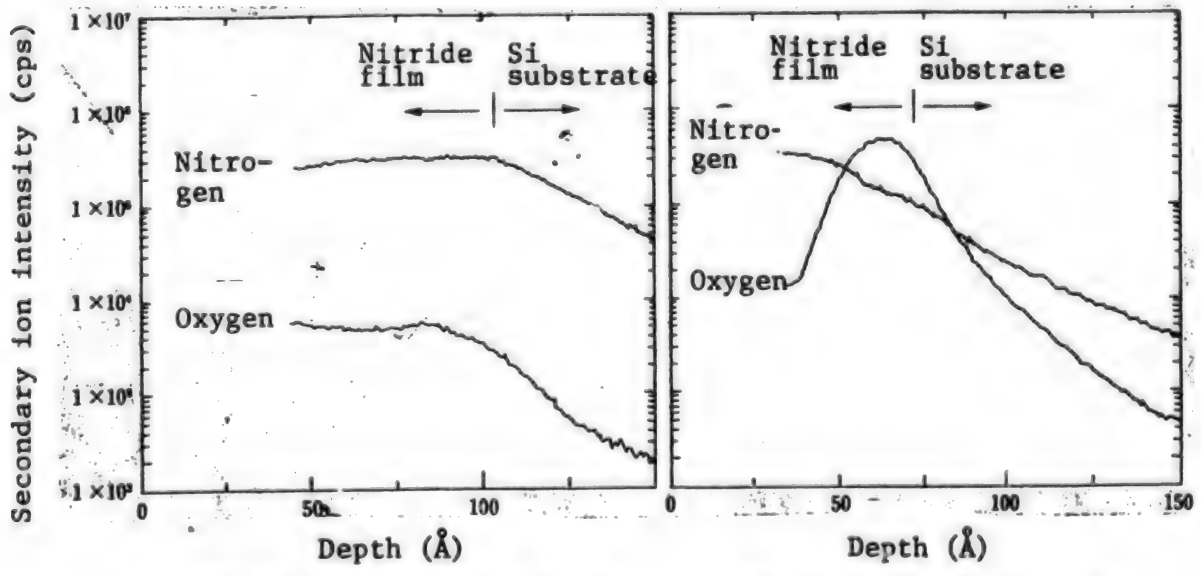


Figure 3. Flow of Continuous Multiple Processing in a Single Module

Key: 1. Natural-oxide film removal; 2. Thermal nitridation; 3. Nitride film CVD; 4. Polycrystalline silicon film CVD

Figure 3 shows the process flow when capacitance nitride film is fabricated by performing several processes continuously in the same module.[6]

Figure 4 shows the result of oxygen analysis in the capacitance film and interface in the depth direction (SIMS). The figure shows that a natural-oxide film layer is observed at the interface between nitride film and



(a) Continuous process including hydrogen baking (b) Without pre-processing

Figure 4. Oxygen Profile on Nitride Film/Silicon Interface (SIMS)

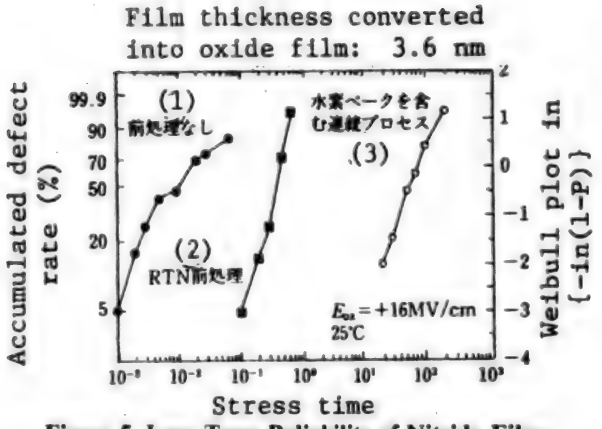


Figure 5. Long-Term Reliability of Nitride Film-Stacked Capacitor (TDDB)

Key: 1. Without pre-processing; 2. RTN pre-processing; 3. Continuous processing including hydrogen baking

silicon in the case where a nitride film is fabricated by stand-alone equipment. Further, the use of continuous, multiple processing using hydrogen baking in pre-processing allows complete removal of the natural-oxide film. This has reduced the leakage current of nitride film-stacked capacitors, and produced a remarkable improvement in long-term reliability (Figure 5).

As described above, continuous, multiple processing in cluster tools or in a single module is a very effective method for fabricating high-quality capacitance film, and an improvement in throughput can also be expected from continuous processing within the same equipment. Further, development of mass-production equipment is desirable as soon as possible. Moreover, since the quality of CVD film varies depending on the purity of the process gas, it is also important to develop gas purification technology along with the equipment improvements.

LP-CVD technology using organic source gas for the deposition of tantalum-oxide film as a highly dielectric film to replace capacitance-insulation nitride film is being developed for 256M DRAMs. The importance of reducing natural-oxide film on the electrode surface of tantalum-oxide film is similar to the nitride film described above.[7] With $SrTiO_3$ and PZT, which are expected to be used as highly dielectric materials, techniques for film fabrication such as the sol-gel, sputtering, and CVD methods are being studied. Expectations are that development of manufacturing methods and equipment suitable for mass production will be available in the near future.

2. Silicon Film Fabrication Equipment

It is expected that the applications of in-situ doped silicon films in devices will expand greatly in the mass-production stage of 256M DRAMs. This expectation is based on the following points: Since decreasing the temperature is a must in the 256M DRAM manufacturing process, the previous technology for thermal diffusion of impurities is of limited use. In addition, it is difficult for current technology to deal with contact poly-Si embedding with a large aspect ratio, and the fabrication of high-quality thin doped silicon film which are required by the progress of integration. In-situ doped silicon film fabrication is promising technology for solving this problem but there are still many technological problems to be overcome for the present. The most important problem is to develop a film with excellent coating which can be used for three-dimensional cylinder capacitor electrodes and microfine contacts. The problem of increased resistance in doped silicon film when fabricating it as thin film has also been pointed out.[8] Furthermore, since the control of natural-oxide film at the interface is necessary when embedding a contact in the same way as when fabricating a capacitance film, cluster tools or multiple processes in the same chamber will also be required.

Recently, fabrication of a special silicon film containing hemispherical grains on the surface (HSG-Si: hemispherical grained Si) has been studied.[9] The HSG-Si film has about twice the surface area of ordinary silicon film and is expected to be applied in capacitor electrodes. Figure 6 [photo not reproduced] shows an example of the use of HSG-Si as an electrode.

To form these hemispherical grains, a clean surface should be maintained so that silicon atoms can migrate freely on the amorphous silicon-film surface. If a natural-oxide film layer is formed on the amorphous silicon-film surface, the migration of silicon atoms would be reduced and HSG-Si would not be formed. Therefore, equipment with low-oxygen partial pressure is also required to prevent natural-oxide film in HSG-Si fabrication.

Oxidation Technology

It is theorized that 256M DRAMs may use gate-oxide films with a thickness of around 80 angstroms. Film thickness at this level is already being developed for use in the gate-oxide films of CMOS and the practical level has already been reached. However, it is still undoubtedly important to advance the improvement of gate-oxide film quality in the future. Consequently, the following discussion deals with the oxidation technology required to promote film quality improvement.

At present, reduction of the interface level, development of oxide film containing nitrogen, reduction of particles, and reduction of metal contamination are being attempted to improve oxide film quality. For these technical subjects, it is necessary to study them from the process side, including cleaning, as well as from the equipment side.

Problems related to the atmosphere when wafers are input to the oxidation furnace have been dealt with often in recent years. Figure 7 shows the difference in oxide-film reliabilities when the oxygen concentration in the nitrogen gas in the furnace is varied.[10] As shown in the figure, the oxide-film quality and reliability vary extensively depending on the oxygen concentration in the furnace.

On the other hand, it has also been reported that, if a wafer with its Si surface exposed experiences a temperature rise or furnace input operation in high-purity nitrogen gas or inert gas, the irregularities on the silicon surface increase and cause deterioration of the electric

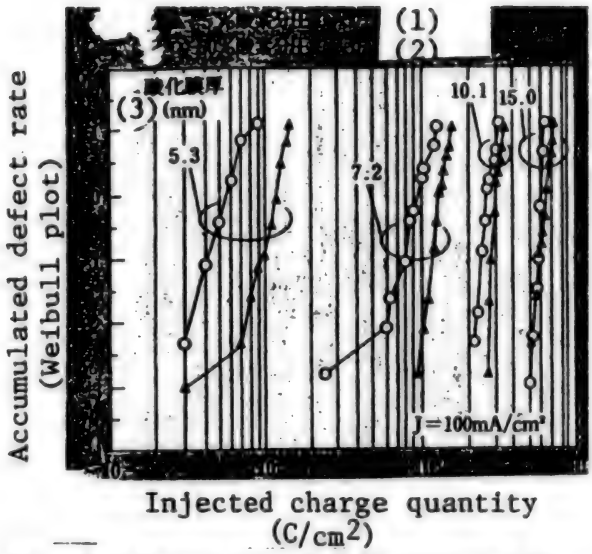


Figure 7. In-Furnace Atmospheric Dependence of Gate-Oxide Film Reliability

Key: 1. Furnace output at 5% oxygen partial pressure; 2. Furnace input at 50% oxygen partial pressure; 3. Oxide film thickness (nm)

properties.[11] Such a problem will not occur if a thin-oxide film is formed by irradiating the silicon surface with UV-O_3 before the wafer is input to the furnace.[11] This indicates that the thin-oxide film protects the surface layer.

As described above, the electrical properties of oxide film are largely variable depending on furnace input conditions. If core tube-type equipment is used in the mass production of 256M DRAMs, it would be advantageous to solve the problems in furnace input without making the equipment more complicated.

It is highly probable that RTP equipment will be applied in the fabrication of gate-oxide film. This is because its cold wall-type structure is expected to be capable of solving the above problems and that problems in throughput may not occur thanks to the gate-oxide film becoming thinner. RTP may also be effective for use in nitrogen-oxide film fabrication because the process gas and temperature can be switched instantaneously.

Conclusion

In the above, the process technologies required for oxidation, diffusion, and LP-CVD equipment in the 256M DRAM generation, and the problems in the equipment have been described. The process technologies for this generation feature the following five points: 1) interface and surface control; 2) continuous processing; 3) lower temperatures; 4) cleaning technology; and 5) complete control of process parameters. To improve the accuracy of such process technologies, it is important to improve control technology based on the understanding of natural phenomena in the manufacturing equipment. Presently, improvement of process accuracy is being attempted by clustering the manufacturing equipment, as this can remove unstable factors originating from outside the equipment. Clustering of equipment is also expected to improve the throughput due to the omission of processes such as cleaning. Conversely, a major source of worry in clustering is a possible increase in equipment failures due to increased complexity. The need here is evident: simplify or standardize the equipment.

In this generation, the selection between batch equipment using core tubes and wafer-level equipment using lamps may be important. Selection according to the processes used may be required. Regardless of the selection, all types of equipment are required to provide low price and high throughput, compatibility with large diameter wafers, and highly accurate control of the atmosphere inside each module.

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Inter-Layer Insulation Film Fabrication Equipment Usable With 256M DRAMs

936C1099F Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 90-95

[Article by Noburo Owada, Device Development Center, Hitachi, Ltd.]

[Text]

Introduction

The higher integration and increased capacity of DRAMs recently progressed at the astonishing rate of four times every three years, but the trend has gradually changed in the past two to three years. This is because of the diversification of market needs and because extensions of current technologies are incapable of dealing with new technological developments in terms of both technology and cost. In particular, while multi-layer wiring technology is needed for the development of memory and logic devices by making the basic processes common, insufficient progress has been made in new technology integrating the micro-wiring/micro-connection holes of memory devices and the increased number of wiring layers/increased chip area of logic devices.

In this report the author would like to introduce his ideas on inter-layer insulation film fabrication technology in the 256M generation and user needs for such equipment from the viewpoint of a process engineer.

Themes for Inter-Layer Insulation Film Fabrication Technology

Flatness requirements of insulation film between wiring layers can be classified into the filling of high-aspect ratio wiring spaces and overcoming wiring height differences as shown in Figure 1. The former requires the plugging of microfine spaces with an aspect ratio of more than 1.0 and the latter requires a global flatness which does not cause any interdependence between wiring width and wiring pattern density. In fact, these issues have been dealt with by realistic solutions at a practical level. Nevertheless, as the level of requirements for these technical solutions has been increasing in importance since the generation of 64M DRAMs, these technological requirements cannot be dealt with by present technology, otherwise the number of process steps would greatly increase along with factors causing the yield to drop.

Table 1 shows the items posing problems if presently used technology for flattening inter-layer films is to be applied in the 256M DRAM generation.

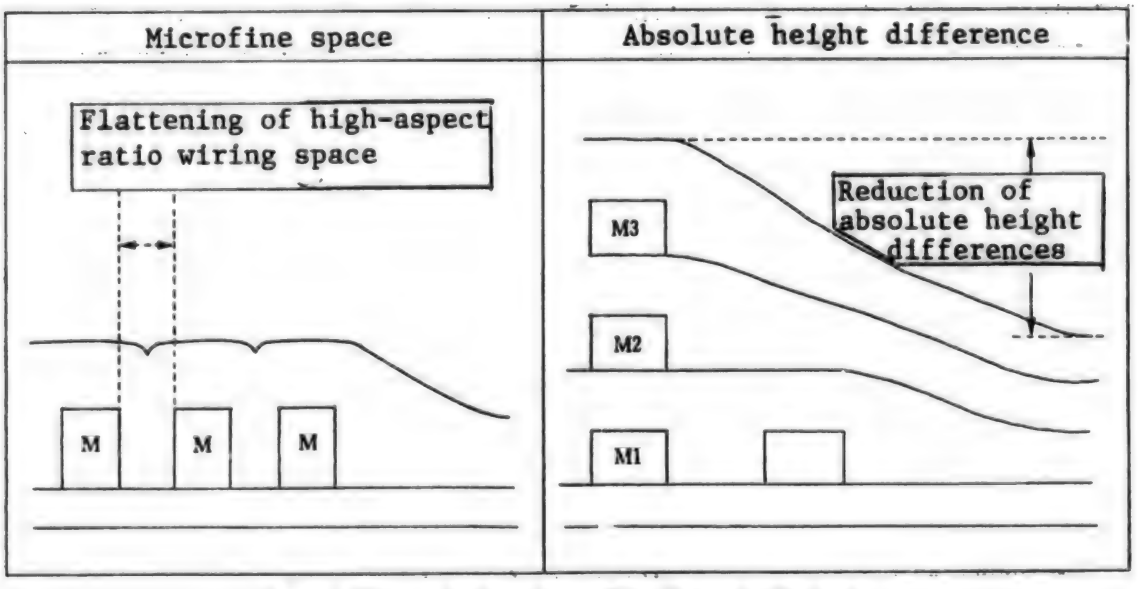

Figure 1. Themes for Inter-Layer Film Flattening Technology

Table 1. Problems in Current Inter-Layer Film Flattening Technology

Flattening technology	Fundamental problems
SOG coating application technology	(1) SOG material which does not need etch-back and which can coat thick film has not been developed
	→ Organic SOG + etch-back process
	→ Complication of process, increase in dust generation potential
	(2) Reduction of wiring space has made it difficult to assure inflow domain in SOG coating
	→ Insufficient resolution of wiring height differences due to denseness/coarseness of wiring patterns (Figure 2)
O_3-TEOS	(1) Flattening by plugging is possible only for specific wiring spaces
	→ Wiring height differences cannot be overcome (Restrictions in design rule such as space width increases)
	→ Combination with other processes is required, causing complication of processes
Sputter-etching combined technology	(1) Plugging characteristics deteriorate following the reduction of wiring space (Figure 3 [not reproduced])
	→ The repetition count of SiO film fabrication and sputter-etching should be increased
	→ Process is complicated and the productivity drops greatly
	(2) Only the inclination angle of height difference can be reduced (45°) but the altitude difference cannot be overcome
	→ Combination with other processes is required, causing complication of processes

The flattening technology used most widely at present is the technology combining SOG-coated film with etch-back, which provides a flatness with a practically permissible level. The biggest problem in this technology or its combination with other existing technologies with regard to microminiaturization is, as shown in Figure 2, overcoming wiring height difference due to the density and coarseness of wiring patterns. This technology basically consists of the fabrication of SiO(1) film used as the base of the SOG coating, coating of SOG, etch-back, and the fabrication of SiO(2) film. However, as microminiaturization decreases the wiring space, the SiO(1) film plugs the wiring spaces. Consequently SOG inflow domains cannot be secured and, in positions where patterns are laid out with high density, the SOG film is deposited thickly above the wiring pattern. This causes insufficient resolution of the wiring height difference due to the density and coarseness of the pattern. To allow this technology to be extended to the 256M generation, new technologies should be developed for the fabrication of SiO(1) film and other SOG-related matters.

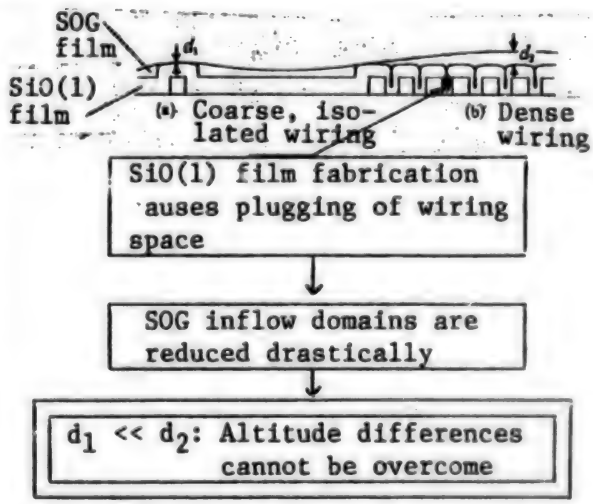

Figure 2. Fundamental Problems in Overcoming Altitude Differences in SOG Flattening Technology

In addition to the use of SOG, flattening technology using ozone-TEOS and that combining sputter-etching are also widely in practice. With the former technology, the film cannot be thick due to its insufficient reliability so the method for fabrication on a plasma-TEOS film with excellent film quality is generally used. As a result, while wiring spaces with specific widths can be flattened by plugging when the film fabrication amount is optimum, the flattening capability is lost with wider wiring spaces. To compensate for this inherent problem of flattening using ozone-TEOS, attempts are being made to use multi-step combinations with other processes or to impose a major restriction on the wiring space in pattern design. With the flattening technology combining sputter-etching, when SiO film fabrication and sputter-etching are repeated alternately, space plugging will be incomplete as shown in Figure 3 [photo not reproduced] and the effective film thickness will vary depending on the wiring space. Figure 3 shows a case using three alternate repetitions. Increasing the repetition count allows widening the process margin, but the result would be impossible to use in mass production. In addition, sputter-etching causes dust generation problems and tends to degrade the components inside the chamber, so it is difficult to improve its stability as production technology. Furthermore, this technology is only capable of reducing the inclination angle between sections with different heights and cannot solve the altitude difference itself, so that multi-step combination with other processes is indispensable to solve the wiring height difference.

Flattening Technology in the Age of 256M DRAMs

Technological developments aiming at plugging of microfine wiring spaces and overcoming the wiring height difference that are required for the 256M generation can be classified into two subjects as shown in Table 2.

Table 2. Topics for Inter-Layer Film Flattening Technology for 256M DRAM Generation

Subject	Item	Development subjects
SOG coating-related technology	Development of coating materials	—Improvement of coating characteristics of patterns with large height differences
		—Improvement of surface mobility during coating baking
		→ Reduction of denseness dependence of wiring pattern
		—SOG material which does not need etch-back and which can be coated in a thick layer
		→ Inorganic SOG, or quality alteration of organic SOG
	Development of coating baking technology	—Control of solvent volatilization rate during rotary coating
		—Film quality improvement by controlling the SOG curing reaction process
		—Measures for prevention of dust from wafer edges/back side
	Development of SiO(1) film fabrication technology	—Reduction of film deposition in wiring spaces
		→ Securing SOG inflow domain (Figure 4)
		—Improvement of film quality on wiring space sidewalls
		→ Securing resistance to cracks and moisture with thin wiring sidewall film thickness
Development of new technologies	Development of ECR-CVD technology	—Basic film fabrication technology (uniformity, film quality, plasma damage, etc.)
		—Control of actual wafer temperature during film fabrication
		→ Heating in initial stage, cooling during deposition
		—Measures for prevention of production of foreign matter derived from objects attached inside the chamber during sputter-etching
	CMP technology	—Achievement of basic performance (polishing rate, reproducibility, throughput)
		—Uniformity and polishing property stability with actual wafers
		—Polishing end-point judgment technology
		—Contamination/foreign matter removal technology, equipment installation environment
	Other new technology	—Establishment of basic technologies → Development in production technology
		Selective TEOS/O_3 CVD-SiO_2 growth technology
		TEOS-H_2O plasma CVD technology, etc.

The first is technological developments based on flattening technology using SOG coating. As described above, application limit of this technology is largely dependent on the SiO(1) film-fabrication technology and SOG-related technology. As shown in Figure 4, by developing: SiO(1) film-fabrication technology which can deposit on peaks to ensure the SOG inflow domains in the microfine wiring spaces while maintaining the film quality (such as resistance to moisture and cracks even on the side walls of wiring patterns); and developing an SOG material which does not need etch-back and which can be coated thickly; and developing an SOG coating technology with improved surface mobility to allow migration from dense pattern areas to coarse pattern areas and so on; the process margin of SOG flattening technology can be improved sufficiently and this technology can be applied continuously in the 256M generation. The second subject is the practical implementation of new technology such as ECR-CVD and CMP (chemical mechanical polishing). ECR-CVD is film-fabrication technology in which SiO film deposition and sputter-etching based on ion impact take place simultaneously. Since the phenomenon as shown in Figure 3 hardly occurs in practice, much is expected of this technology in its capability of plugging high-aspect ratio spaces by itself. Figure 5 [photos not reproduced] shows cross-sectional SEM micrographs of an example of the application of ECR-CVD. As ECR-CVD leaves projections on the wiring patterns, additional processing to remove them is required. The technical problems with ECR-CVD technology include damage, wafer temperature control, foreign matter countermeasures and productivity, as well as the basic properties of the film. CMP technology is attracting strong attention as a new flattening technology but its practical implementation presupposes inter-layer insulation-film fabrication technology which can plug microfine wiring spaces. The development issues of CMP include uniformity, polishing, control, influence of density differences on the pattern, removal of contamination and foreign matter and the equipment installation environment. Its potential as production technology with high process accuracy is being studied also, taking the thickness variations of the silicon wafer itself (around 20 μm) and warp with actual wafers (around 100 μm) into consideration.

As described above, two promising flattening technologies for the 256M generation are technologies based on SOG, and ECR-CVD and CMP. However, these two technologies may be used by selecting one according to the level of the individual flattening requirement. On the other hand, new technologies are being developed which can plug microfine spaces and overcome wiring height differences simultaneously in a single process.[1,2] What

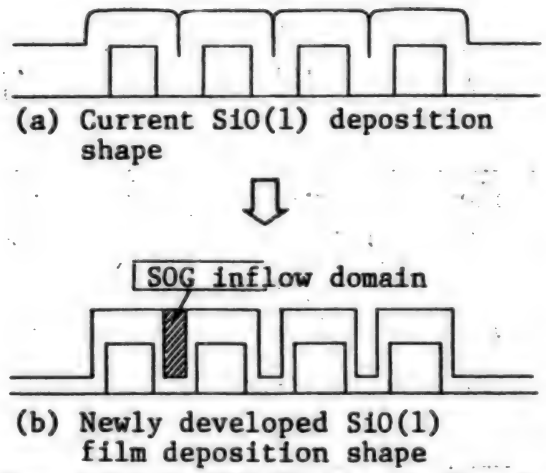

Figure 4. Suitable SiO(1) Film Deposition Shape for SOG Flattening

the process engineers are really seeking is such a single-process breakthrough, and it will take such to achieve an effective simplification.

Perspective of Inter-Layer Insulation Film Fabrication Equipment

As described in the above, flattening technology in the 256M generation is following the sequence of searching for a breakthrough technology while maintaining a development strategy based on existing technology, and covers a wide range of technologies including plasma CVD, coating, ECR-CVD, polishing and others. Therefore, depending on what kind of process is selected, the equipment used will vary and hardware requirements will also differ. Basically, equipment which can assure reproducibility and stability for the resolution of the processes described above is urgently required.

From the aspect of production technology, the processing capability, including the operating ratio and dust prevention measures, will be more important than ever. The operating ratio should be considered as a reduction of the time during which wafer processing is impossible, rather than a reduction of failure time. That is, maintenance and inspection time, including the exhaust/harm removal systems, should be counted in the time wafer processing is impossible.

Dust prevention measures will be based on previously acquired technology such as dust-free robot arms and frictionless valves, and foreign matter reduction measures should not be dependent on existing knowledge or process, but be dealt with from an aspect of hardware such as the component materials or equipment concept. In this context, self-cleaning of the process chamber, which has recently been put to general use should be treated as an important process technology. Self-cleaning itself is an important plasma process and a design cognizant of in-plane uniformity, end-point judgment technology, and matching with other components inside the chamber will be required more than ever in the age of 256M DRAMs.

As for recent trends in general production facilities, while advances in equipment are being promoted through the development of automated equipment, wafer-level handling, cluster tools and intelligent equipment incorporating process monitoring and data communications functions, the requirements for cost reduction and energy saving are also growing rapidly. Certainly, inter-layer film flattening technology presupposing a multi-step process combining plasma-TEOS film, ozone-TEOS film, sputter-etching etc., automation, wafer-level processing, clustering and the use of artificial intelligence for achieving process accuracy, will be necessary. But these will result in a drastic increase in equipment cost and virtually ignore process simplification. What is required in the age of 256M DRAMs is not an apparent simplification such as the clustering of complicated processes, but completely new technology to simplify the processes.

Conclusion

In recent years, the development of LSIs and reduction of production costs have become critical requirements determining the survival of the semiconductor industry, and the technological requirements for flattening of multi-layer wiring are also getting more and more severe. In this situation, both equipment manufacturers and device manufacturers fully recognize that processes based on a combination of existing technologies cannot address the industry of the future.

Therefore, improvements of present technologies can deal with problems from the 16M generation to the beginning of the 64M generation but, when the 256M generation is considered, both equipment and device manufacturers will have to stress the simplification of technologies themselves or the implementation of new technologies that allow simplification, rather than the pursuit of apparent simplifications by clustering or automation of multi-step processes. Conceiving new approaches to 256M production is expected to give a new vitality to inter-layer insulation fabrication technology in the age of 256M DRAMs.

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Metal CVD Equipment Usable With 256M DRAMs

936C1099G Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 96-99

[Article by Tatsuru Hara and Takayuki Ohba, Basic Process Development Dept., and Michiari Kono, Process Integration Dept., Fujitsu, Ltd.]

[Text]

Introduction

Device design, process, and equipment development have started for 256M DRAMs, the mass production of which is expected to start in the year 2000. With 256M DRAMs, which are expected to require ¥100 billion to ¥200 billion for R&D and a few times more for mass

production, the point is how to make it possible to produce efficiently while minimizing plant and manufacturing equipment investments.[1] In general, this is being attempted by using the same manufacturing equipment to produce several generations of devices and refining existing process technology. However, with regard to quarter-micron devices, limits in manufacturing technology and processes have already been seen, particularly with multi-layer wiring.

This report describes the present status of metal CVD technology for multi-layer wiring and the necessary equipment configuration for it.

Problems in Multi-Layer Wiring

Table 1 shows the problems to be studied for multi-layer wiring used with 256M DRAMs.

Table 1. Problems To Be Studied for Multi-Layer Wiring Technology for 256M DRAMs

Technology	Material	Items
Wiring	Al	Prevention of wire breakages due to migration
	Cu	Stable supply of liquid source
		Patterning method
		Throughput improvement
		Oxidation prevention
	Blanket W	Throughput improvement
		Particle reduction
		Film separation prevention
		Stress reduction
		Resistance decreased
	TiN	High-coverage film fabrication
		Particle reduction
		Decreased temperature
Plugging	Blanket W	Process reduction
		Particle reduction
	Selective W	Surface processing technology
		High selectivity

As device microminiaturization advances, migration breakages of Al wiring will be significant. Meanwhile, CVD-single-crystal Al recently developed is attracting attention for its resistance to wire breakages.[2] High melting point metals such as W and Cu are expected to be used as wiring materials to replace Al because these metal atoms hardly cause migration. The problems studied for blanket W wiring include increased throughput, particle reduction, stress reduction, and decrease of resistance. Since the current density increases as the wiring becomes finer, the generation of Joule heat cannot be disregarded, with W having a higher resistance than Al. It was recently found that W with a resistance of about 7 microhm-cm can be formed into film-by-film fabrication using diborane.[3] On the other hand, it is essential to use bond layers to prevent the separation of blanket W and, due to the physical limit of TiN coverage by sputtering, the CVD of TiN is being studied in this context. CVD-TiN with high coverage and low temperature can be used in Al multi-layer wiring and is expected to be used as plugging technology replacing W. Film fabrication utilizing hydrazine reduction[4] was also developed recently. It is expected that composite wiring technology of CVD-TiN and CVD-W will be used in next-generation processes. With wiring formation by CVD-Cu,[5,6] problems include the method of supplying a stable liquid source, etching, Cu oxidation and so on.

Contact holes and via holes can be plugged with blanket W or selective W, which are being studied from the viewpoints of process and cost. Since selective W makes positive use of chemical differences on the surface, a cleaning process is used before film fabrication to remove natural-oxide film. Selective W should guarantee selectivity for a variety of inter-layer films. Plugging with blanket W, at least three processes, TiN, blanket W, and etch-back, are necessary so stacked wiring should be advanced, resulting in a cost disadvantage in the age of 256M DRAMs where productivity is especially important. Therefore, the simplest and most effective method may be to use selective W for plugging, and form multi-layer wiring by sputtered Al.

Clustering of Equipment

To improve the reliability of multi-layer wiring for 256M DRAMs to a similar or better level than existing devices, plugging and wiring using CVD films with excellent coverage or stacked wiring combining CVD film and sputtered film may be necessary. To fabricate low-resistance contacts, interface control is important to remove natural-oxide film and contamination on the contact surface and form a clean surface with good

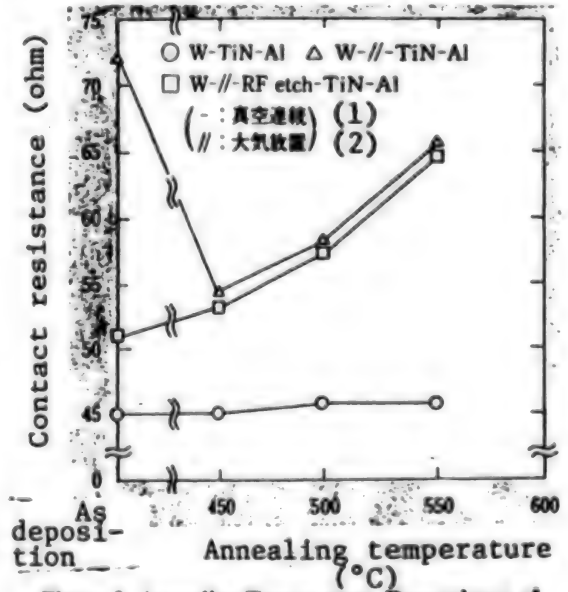

Figure 2. Annealing Temperature Dependence of Contact Resistance

Key: 1. In vacuum, continuous; 2. Standing in atmosphere

reproducibility. Particularly, attention should be paid to residual oxygen or moisture when fabricating Al or Cu films. From these viewpoints, studies are being conducted into the combination of sputtering and CVD and into clustered equipment consisting of several sputtering chambers or CVD chambers.[7]

Figure 1 [photos not reproduced] shows the effects of post-processing and continuous processing in selective W film fabrication.[8] Films can be formed on wafers which have been transported in vacuum after dry pre-processing, but cannot with conventional wet pre-processing using HF/H_2O. Therefore, selective W must be combined with dry pre-processing, which can be achieved with clustered equipment. Figure 2 shows the contact resistance when sputtered TiN and Al are formed into films continuously in vacuum or discontinuously (with a period of standing in atmosphere) after W film fabrication.[9] Contact resistance in the case of in-vacuum continuous-film formation is lower than that of standing in the atmosphere between processes. This is because the W surface is oxidized in the atmosphere in the case of discontinuous film formation, and shows the effectiveness of in-vacuum continuous processing.

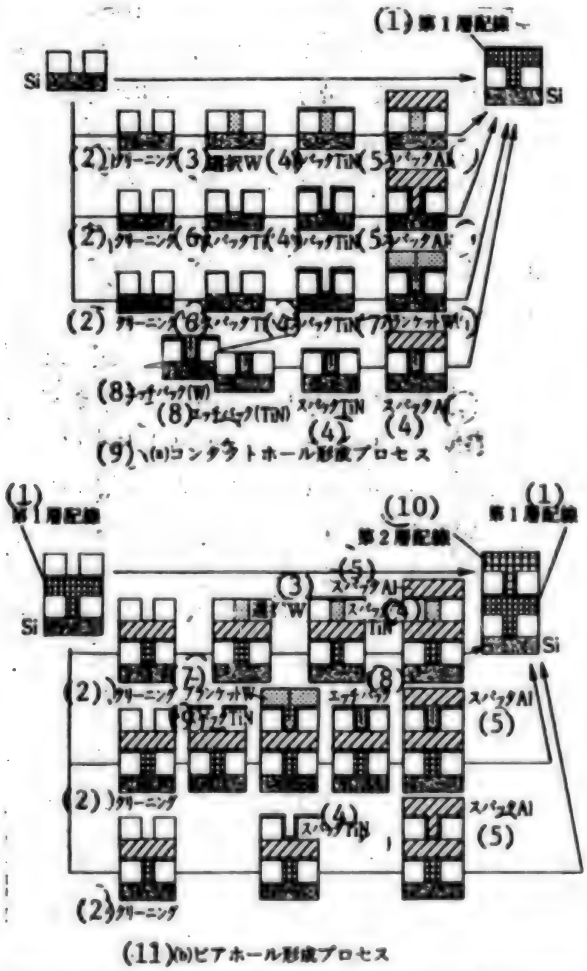

Figure 3. Examples of Multi-Layer Wiring Fabrication Processes

Key: 1. 1st-layer wiring; 2. Cleaning; 3. Selective W; 4. Sputter TiN; 5. Sputter Al; 6. Sputter Ti; 7. Blanket W; 8. Etch-back; 9. (a) Contact hole fabrication processes; 10. 2d-layer wiring; 11. (b) Via hole formation processes

Figure 3 shows typical examples of multi-layer wiring processes, those for contact hole plugging and for via hole plugging.[10] To use the reflow of sputtered Al for plugging, a three-chamber configuration is required including the base TiN and annealing chambers. Plugging with selective W is based on a two-chamber configuration including a pre-processing chamber. Plugging with blanket W requires four or five chambers from pre-processing until etch-back so the scale of clustered equipment becomes large. The etch-back process is not necessary when blanket W is used directly for wiring. As seen above, there are several available process combinations, and it is important for the fabrication of multi-layer wiring to select low-cost processes which emphasize productivity.

On the other hand, the implementation of clustered equipment is an approach for minimizing so-called process dead time by increasing throughput by means of several identical chambers as well as composite processes, the number of chambers based on the processing time of each process. This makes the use of modular chambers important. Figure 4 shows typical examples of the layout of the chambers of clustered equipment.[11]

No. of chambers	Radial-type	Linear-type
2		
3		
4		
5		
6		

Figure 4. Examples of Chamber Configuration of Clustered Equipment

Advantages of Clustered Equipment, Future Topics

Table 2 shows the advantages of metal CVD, or generally speaking, the clustering of wiring equipment, and future topics. The biggest advantages include the maintenance of the fabricated film surface with high reproducibility, the prevention of contamination, and the reduction of processing time.

Table 2. Advantages of Equipment Clustering, Future Topics

Advantages	Topics
Maintenance of deposited surface with high reproducibility through vacuum transportation	Prevention of cross-contamination between sputtering and CVD
Prevention of foreign matter adsorption or contamination through continuous processing	General reliability of equipment
Reduction of processing time required for several processes	Soft reliability of composite process
Reduction of footprint in clean room	Development of several processes as a total process
Possibility of combining desired process chambers with a high degree of freedom	Reduction of cost
	Increase of throughput

It is said that more than 80 percent of the defects with 64M to 256M DRAMs are attributed to particles or metal contamination on the wafer. Particles and contamination are produced in the film-fabrication chambers or during wafer transportation and are influenced by the cleanness of the manufacturing line. In the future, because the environment of the manufacturing line will be "super-clean," particles and contamination will mainly be due to the equipment. It is estimated from the above that more than 90 percent of the drops in yield of 256M DRAM-class products would be due to particles and contamination.[12] In consequence, therefore, the problems in the clustering of equipment will include how to reduce dust production in individual film fabrication chambers and the transportation system. Particularly, with blanket W, if bonded layers are fabricated from sputtered TiN, W film separation from the periphery may occur depending on the TiN film state and the W above the susceptor will tend to be the source of particles. This will be dealt with by the use of uniform TiN film or a method for prevention of W film formation around the wafer by adjusting the mechanical clamp of the wafer or the gas flow. Cleaning equipment is also being studied. On the other hand, with the combination of the Al sputtering and CVD chambers, the trend is the use of ultrahigh vacuum. Optimization of the transportation pressure is necessary from the viewpoints of cross-contamination and particles. In this way, the clustering of equipment allows a combination of processes but requires high system reliability and excellent maintainability. This is because the increase of equipment size inherently degrades reliability and, should the equipment fail, the wafer process itself would be impossible. Therefore, the equipment's reliability and operation ratio will be important bases for judging equipment usable with 256M DRAMs.

Conclusion

Increase in the scale of device integration has made plant investment so huge that profitability has become questionable. As a result, 256M DRAMs require rather simplified processes to reduce production costs. Technology combining plugging with selective W and sputtered Al is considered suitable for economical multilayer wiring fabrication, along with a high manufacturing equipment operation ratio. On the other hand, wafer size increase, process composition and film stability requirements make wafer-level reaction chambers the most practical and clustered equipment is suitable to use them. While the selection of processes which are realistic from the viewpoints of device and cost is necessary to implement the above, how clustered equipment should be developed has not been established at present because there are still various proposals on the chamber configuration to be used. Therefore, to implement multi-layer wiring for 256M DRAMs at low cost, the equipment should be implemented based on specific data to prevent over-specification, while presupposing the use of high-reliability wiring. To achieve this end, the integration of process development and equipment development will become more and more important.

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Sputtering Equipment Usable With 256M DRAMs

936C1099H Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 100-103

[Article by Yukio Kanno, VLSI Laboratories, Sony Corp.]

[Text]

Introduction

Semiconductor devices are steadily increasing in scale, and 256M DRAM quarter-micron rule devices are currently being developed. Microminiaturization and the increased scale of integration necessary to deal with this are gradually increasing the importance of wiring technology. This is because the wiring process has become the process determining the yield and reliability of devices. The recent trend is that the wiring structure itself is complex, in addition to microminiaturization and the attendant increase in the number of layers of wiring. This is apparent specifically with plugging technology for filling fine contact holes and the stacking with high melting point materials to assure the reliability of Al wiring.

Sputtering has played an important role in the fabrication of Al wiring. Although CVD is gradually penetrating the domain of metal film fabrication, sputtering technology may remain necessary as long as Al wiring is used because Al is a very active material and sputtering is beneficial for obtaining good film quality from such a material. Since sputtering equipment supplanted deposition equipment in metal film fabrication, it has experienced various technical innovations including wafer-level processing and the use of multiple chambers. After composite processing with CVD or annealing has almost reached a practical level, almost all of the present sputtering equipment is being made with cluster tools.

This report describes the configuration and functions of the sputtering equipment required for manufacturing 256M DRAM-class devices, but in this changing environment it is difficult to present the total picture. The report first describes the dissatisfaction of users concerning existing sputtering equipment, then considers some of the functions required for future sputtering equipment.

Problems in Equipment Configuration

First, let us consider the equipment configuration. To assure uniformity in film thickness, sputtering needs a target with 1.5 to 2 times the diameter of the wafer. For example, as shown in Figure 1, a target with a diameter of 300 to 360mm is used with an 8-inch diameter wafer. This necessitates a larger process chamber than CVD equipment. Following the use of multiple chambers and wafer size increase, the equipment now has a very large footprint, making it almost impossible to install adjacent to other process equipment. Apparently, equipment manufacturers are unaware of this problem. Users need equipment with a body depth of less than two meters. It is also desirable to reduce the size of auxiliary equipment such as the power supply unit, or to stack it to reduce its footprint.

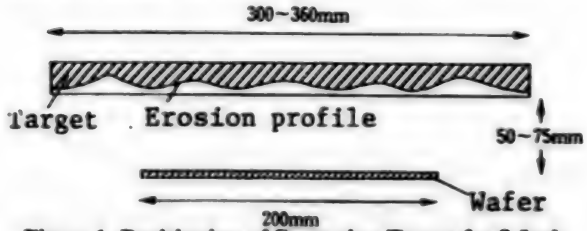


Figure 1. Positioning of Sputtering Target for 8-Inch Wafer

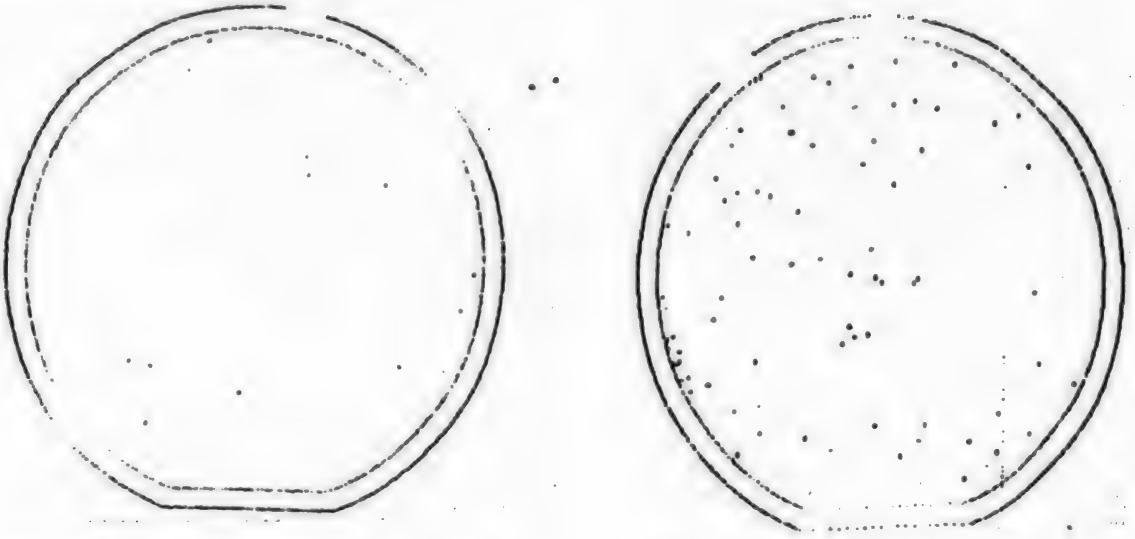
Since layered wiring started to be fabricated using multi-chamber equipment, throughput has halved compared to conventional film fabrication using Al alone. What is worse, the complexity of multi-layer wiring and layered wiring has increased the number of sputtering processes. This drives the urgent need for multi-chamber sputtering equipment with high throughput. To increase throughput, it may also be necessary to review the semi-independent chamber system using plate transfer, without continuing the use of arm transport systems.

Problems in Basic Functions

Next, consider some of the basic functions of the equipment. Up to the present, the performance of process equipment has often been evaluated under simplified conditions that differ from actual operating conditions. The simplified conditions do not emulate controlling the actual device manufacturing process. This evaluation method for controlling or monitoring the status of actual film fabrication itself needs evaluation.

Particle reduction is the most important topic in sputtering equipment for the 256M DRAM generation. While clean-room technology is advancing, the reduction of other factors causing particles in manufacturing equipment is not sufficient. Especially, following the microminiaturization and multiple layers of Al wiring, particles from the sputtering equipment have become the main factor degrading yield. In general, particles attached to wafers have been evaluated by simply examining the transport operation. However, since it was found that particles are also produced during film fabrication, evaluation covering the film fabrication process has become essential. Measuring particles had been difficult because metal films have high reflectivity and large surface coarseness but, as shown in Figure 2, measurement is possible even when metal films are used. Of course, equipment which can guarantee a low particle count even with film is desirable.

Major sources of particles in sputtering equipment are the wafer transportation system and the targets and anti-deposition plate in the process chamber. With regard to the wafer transportation system, it has been proposed to apply vertical or face-down transportation, but the correct method to reduce particles may be to simplify the wafer transportation system rather than to rely on wafer orientation. With regard to particles from the target, they can be reduced greatly by using full-face



(a) Al-1% SiO, 1 μm thick: 15 particles of more than 0.3 μm

(b) Ti 30 nm thick, TiON 70 nm thick: 65 particles of more than 0.3 μm, 128 of more than 0.2 μm

Figure 2. Examples of Measurements of Particles With Metal (on 125mm diameter wafers)

eroded cathodes.[1] Dust from the anti-deposition plate or clamping mechanism is also a source of worry. In-situ cleaning is used in practice with CVD equipment but practical use of in-situ cleaning with sputtering is deemed difficult. Problems include attaching of the film over a wide area of the anti-deposition plate and the adverse influence of reactive gas on the fabricated film quality. Improving the bonding force by plasma conditioning or reducing thermal stress by maintaining the anti-deposition plate heating temperature have been proposed, but a more essential improvement is desirable. Figure 3 shows the results of composition analysis of particles detected after film fabrication with Ti and TiON. SUS and SiO_2 particles are derived from the transport system and Al and TiON particles are believed to be produced in the process chambers, though the specific positions cannot be identified.

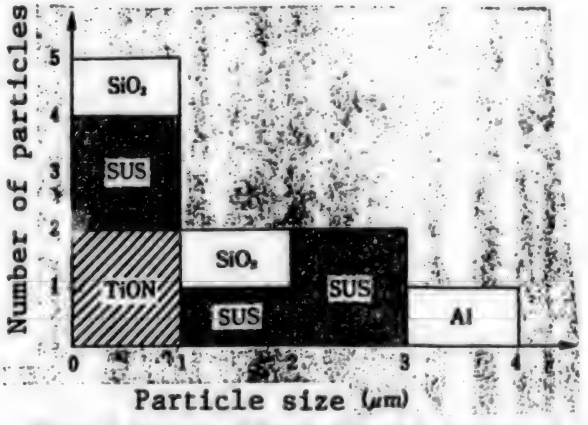


Figure 3. Example of Result of Particle Analysis of Sputtering Equipment

With wafer heating, much sputtering equipment is now capable of heating the stage up to 600°C, and temperature distribution is also being improved. The technology can be considered to have reached the practical level when application in high-temperature sputtering, which plugs contact holes by flowing Al, is taken into account.[2] However, while the temperature during film fabrication and its distribution are most important, they are not controlled completely for the present because of the difficulty in temperature measurement during film fabrication. It is desirable to monitor the temperature during film fabrication, control it within 10°C from the target temperature, and control the temperature distribution over the wafer within 10°C. Gas heating by flowing gas between the wafer back-side and stage is advantageous for preventing an excessive temperature rise during film fabrication. To improve temperature uniformity it may be necessary to divide the stage into several areas and apply independent temperature control to each.

With the degree of vacuum, a base pressure of the order of 10^{-9} Torr is now available in mass-production machines thanks to their ultrahigh vacuum capability. An ultrahigh vacuum is necessary for fabricating high-reliability Al wiring with a large grain diameter and good orientation, and to stabilize the process of high-temperature sputtering. Nevertheless, with substrate heating of around 500°C required for high-temperature sputtering, for example, a vacuum of the order of 10^{-9} Torr has not been achieved due to increased degassing

from the chamber. It is desirable that equipment achieve a base pressure of the order of 10^{-9} Torr, even used for heated film fabrication at 600°C. However low the base pressure, it is still meaningless if there is any degassing from the target and its surroundings. Figure 4 shows that the peak of H_2 rises when Al film fabrication is started. This is because moisture is emitted from the target surroundings; this reacts with Al and H_2 is left as a result. Such degassing should also be reduced.

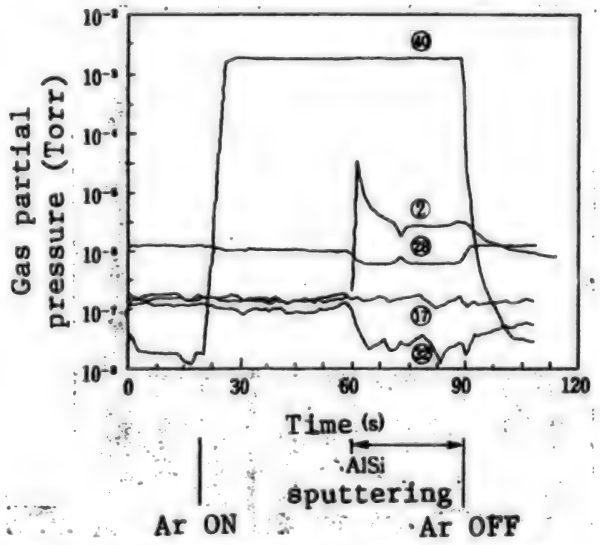


Figure 4. Analysis of Gases in Al Film Fabrication (with intentional atmosphere leakage of 1 x 10^{-6} Torr)

In the figure, (40) is the Ar sub-peak, (2) the H_2 sub-peak, (3) the N_2 sub-peak, (17) the H_2O sub-peak, and (32) is the O_2 sub-peak

Additionally, film fabrication rate monitoring, which has been possible with batch-type systems, is not possible when a wafer-level method is used. Considering the increasing necessity of fabricating thin films such as reflection prevention film with high controllability, the revival of this function is desirable.

Desirable New Functions

The following describes the new functions desirable for sputtering equipment.

The first desirable function is the improvement of coverage. In the age of 256M DRAMs, contact holes will have diameters of 0.3 μm and the aspect ratio will be around 3. In such a case, ordinary sputtering may be able to achieve only a small percentage of coverage, which is insufficient even for bonded layers of blanket tungsten. Coverage can be improved by increasing the vertically incident component. A solution for this is collimated sputtering, but this method is difficult to use due to collimator blocking and particle production problems. Another possible method is to reduce the scattering of sputtered particles by decreasing sputtering gas pressure. As ECR sputtering[3] has been proposed as a specific method, the announcement of a practical machine is awaited. It is also effective to decrease oblique incident components from the target surroundings by decreasing the target diameter or by increasing the distance between the target and wafer. But, this is a trade-off with the film thickness distribution in the wafer.

Another attractive new function is combining with CVD or annealing. It is estimated that microminiaturization of the contact holes would lead to the necessity of continuous processing to avoid oxidation due to atmospheric exposure in order to secure the ohmic contact. Specific merits of this method have already been reported[4] but further study may be required on the inevitability of using it on a manufacturing line.

Conclusion

In the manufacturing of semiconductor devices, sputtering is increasing in importance as a process determining yield and reliability. However, existing sputtering equipment in which the use of cluster tools is advanced poses problems in terms of footprint and throughput. Since particles will be a more important problem following a microminiaturization, reducing them will be the most important topic in the device manufacturing of 256M generation DRAMs. The advantages of composite processes which are attracting attention require further study.

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256M 0.25 Micron EB Direct Drawing Technology

936C1099I Tokyo SEMICONDUCTOR WORLD in Japanese Aug 93 pp 33-37

[Article in the "Technical Report" pages by Ken Nakajima, Yoshikatsu Kojima, Satomi Hirawa, and Naoaki Kashiwazaki, ULSI Device Development Laboratories, NEC Corp.]

[Text]

Introduction

The development of advanced devices at the 256M DRAM level requires technology for the fabrication of patterns of 0.25 μm or below (with an accuracy of +/- 0.05 μm). For pilot fabrication, it will be necessary to provide stable microfine pattern fabrication technology (equipment, processes, etc.) in a few months. At the present stage in which photoexposure (i-ray, KrF, + resolution improvement) technology which is fully usable below 0.25 μm has not been established yet, electron beam (EB) direct-drawing technology, which is capable of drawing microfine patterns and is not restricted by chip size, is considered the only lithography technology which can provide stable processing in this

domain. Usually, the following are considered the major issues of the EB direct-drawing technology.

(1) EB equipment technology: Analysis and improvement of drawing accuracy, improvement of throughput, and stabilization of operation.

(2) Resist process technology: Selection of resist, optimization of process conditions, and countermeasures against charge-up.

(3) Pattern data processing technology: Technology for conversion of massive data, correction of proximity effect.

These are universal technological issues that have been tackled for more than a decade; technologies have been developed and optimized for each generation and applied in prototyping advanced devices.

Recently, we developed and optimized these technologies and applied the results to prototype a 256M DRAM.[1] In this report, we will introduce 0.25 μm EB direct-drawing technology, detailing the analysis and improvement of drawing accuracy with regard to drawing equipment, optimization of process conditions with resist processing technology, and correction of the proximity effect by pattern data processing technology.

EB Equipment Technology—Analysis and Improvement of Drawing Accuracy

To secure the drawing accuracy required for 0.25 μm processes, analysis and evaluation of the accuracy of each part of the equipment is necessary along with the study of accuracy improvement based on the results of the analysis. Variable-shaping EB equipment[2] used for our prototyping provided the drawing accuracy analysis results shown in Table 1, where the improvement of mark detection accuracy with the largest error is essential.

Table 1. Results of Drawing Accuracy Analysis of Variable-Shaping EB Equipment

Factors	Drawing error 3 (m)	
	Before improvement	After improvement
Column system	≤ 0.017	[left arrow]
Stage system	≤ 0.084	≤ 0.038
Deflection system	≤ 0.030	[left arrow]
Calibration system	≤ 0.040	[left arrow]
Mark detection system	≤ 0.046	≤ 0.020
Environment	≤ 0.017	[left arrow]
Overall	≤ 0.110	≤ 0.070

The EB equipment uses symmetrical correlation computation applying a correlation operation,[3,4] and features the capability of highly accurate detection even with low S/N signals and low dependence on the shape of marks. But the detection accuracy is largely variable depending on the value of correlation operation parameter W (correlation operation width). Therefore, to minimize variations in detection accuracy, we developed a technique for optimizing operation parameter W.

Figure 1 shows the W optimization technique that we developed.[5] First, to improve the S/N of input signal Y(i) (the primary differential signal in mark detection), autocorrelation processing is performed and output correlation signal Z'(i) is obtained. Then, from the signal peak width of Z'(i) with improved S/N, optimum correlation operation parameter W is obtained from the following formula:

$$W = W_0 + \Delta W$$

Here, ΔW is the beam width when a mark is detected. The use of this technique can improve the mark detection accuracy from 0.046 μm (3 σ) to 0.020 μm (3 σ). In addition, overall drawing accuracy was improved by improving the stage-moving accuracy. These improvements have made it possible to reduce the calculated overall drawing accuracy below 0.070 μ (3 σ), assuring the drawing accuracy necessary for use of the 0.25 μm rule.

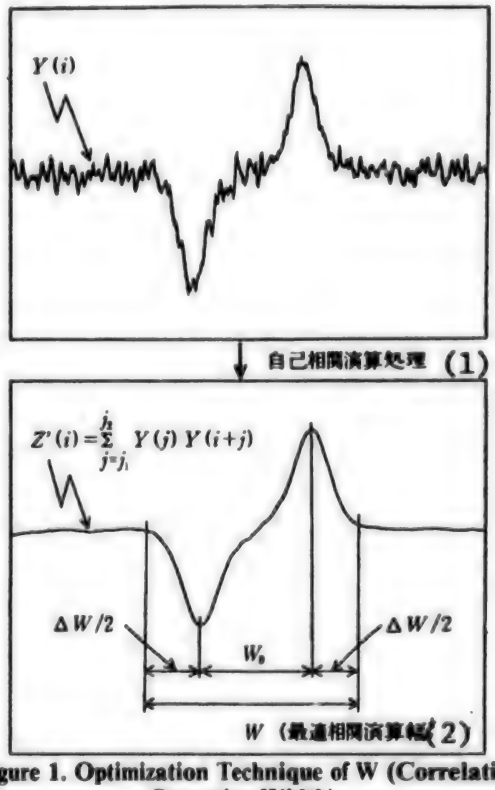

Figure 1. Optimization Technique of W (Correlation Operation Width)

Key: 1. Autocorrelation operation processing; 2. (Optimum correlation operation width)

Figure 2 shows the alignment accuracy in the actual prototyping of a 256M DRAM. It refers to the accuracy of the word-line layer with respect to the device-separation layer. The accuracy is good on both the X and Y axes, sufficiently within the alignment margin required from the device structure. Similar alignment accuracy results were also obtained with other layers by previously optimizing the correlation operation parameter for each EB drawing layer, within 0.075 μm (3 σ) which is almost the identical level to the calculated accuracy.

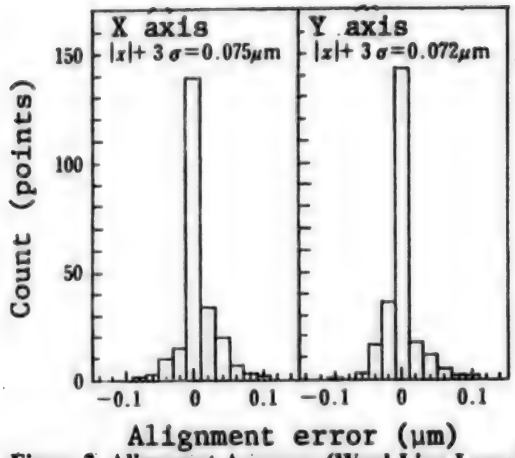

Figure 2. Alignment Accuracy (Word-Line Layer)

Resist Process Technology—Optimization of Process Conditions

With EB direct drawing, electrons lose energy when they are scattered in the resist, and this energy forms a negative or positive image by causing chemical reactions among the resist molecules. Therefore, electron scattering in the resist is the most important factor governing the shape of the resist. Because the prototype EB equipment used an accelerating voltage of 20 kV, the resist film thickness should be decreased to reduce the influence of forward scattering. However, thin resists cannot cover the height differences in the device and are not sufficient for use as the mask in etching. Actual prototyping was based on a multi-layer resist process. A single-layer resist process was also used in some instances for reducing the TAT.

When a multi-layer resist process is used, it is essential to optimize the thickness of the organic film in the lower layer. Previously, the lower-layer organic film had a large thickness (1 to 2 μm) to reduce the influence of backscattering from the wafer. However, when drawing patterns at the 0.25 μm level of the 256M DRAM class, the aspect ratio rises during organic film etching, causing a size shift, pattern tilting, and shape deterioration. In short, the minimum required thickness of organic film is determined by the absorption of height differences, resistance to etching, and influence of backscattering.

We first studied the thickness of the lower-layer organic film and the influence of backscattering by simulating energy accumulation.[6,7] As shown in Figure 3, the thickness of the lower-layer organic film hardly influences the contrast of the distribution of the electron accumulation amount (at the interface with SOG film). This result shows that the thickness of the lower-layer organic film can be optimized by considering only the thickness of the etched material and the height difference on the wafer in every EB drawing.

Figure 4 [photo not reproduced] shows the bit-line patterns of SAL601 negative-resist prototype with a multi-layer resist process.

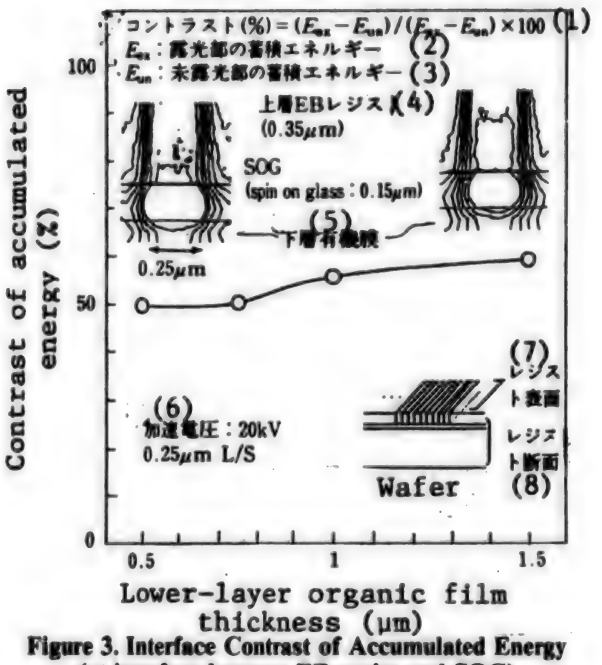

Figure 3. Interface Contrast of Accumulated Energy (at interface between EB resist and SOG)

Key: 1. Contrast (%) = $(E_{ex} - E_{un})/(E_{ex} - E_{un} \times 100$; 2. E_{ex}: Accumulated energy of exposed section; 3. E_{un}: Accumulated energy of unexposed section; 4. Higher-layer EB resist (0.35 μm); 5. Lower-layer organic film; 6. Accelerating voltage: 20 kV; 7. Resist surface; 8. Resist cross-section

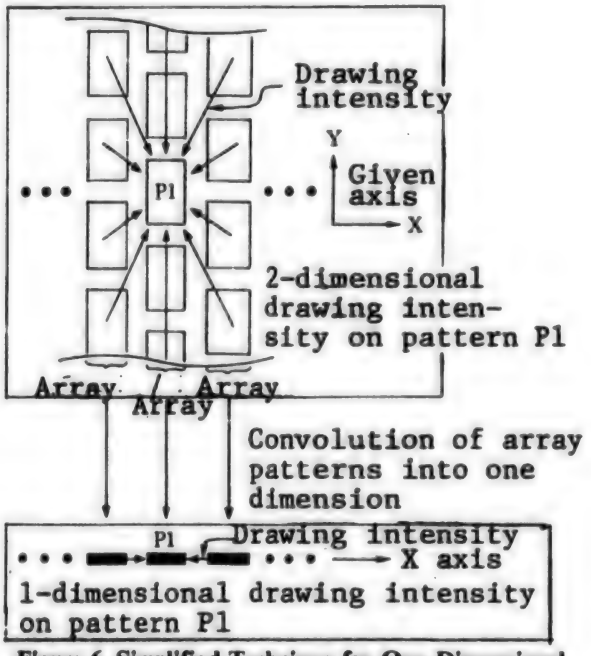

Figure 6. Simplified Technique for One-Dimensional Processing for Correction of Proximity Effect

The single-layer resist process can be applied in prototyping in the case where the height difference on the wafer is small, the pattern is coarse, and the selectivity ratio between the etched film and resist is sufficient. As the single-layer resist process allows the TAT and etching count to be reduced, it makes it possible to minimize size variations.

In actual prototyping, the single-layer resist process was applied with bit-line and capacitance contacts. As shown in Figure 5 [photos not reproduced], contacts were fabricated with reasonable accuracy in both (a) the cell-array section and (b) the peripheral-circuit section. This is assumed to be possible by a small mutual proximity effect attributable to the relatively coarse drawing pattern and by the wide exposure margin of the ZEP520 positive resist used.

Pattern Data Processing Technology—Correction of Proximity Effect

For the fabrication of microfine patterns of the 0.25 μm class using EB direct-drawing technology, it is essential to correct the proximity effect which degrades the drawing accuracy. Therefore, when we converted the design data into data formatted for the EB equipment, we developed a data conversion system which can correct the proximity effect at the same time as the two-level data compression processing.

This correction processing is based on the two-dimensional self-consistent method using the EID (energy intensity distribution) function,[8] and also uses contour processing and rectangle redivision processing. Also, we specially developed a vector processing system using an SX-2 supercomputer and a simplified one-dimensional drawing intensity calculation technique to decrease conversion time (CPU time).

Figure 6 shows the basic concept of the one-dimensional processing technique. In case identical patterns are developed infinitely (beyond the backscattering domain) in the direction of an axis (Y axis), the mutual proximity effect (drawing intensity) in the axial direction can be considered constant. Therefore, because the intensity drawing on the pattern to be corrected (required when

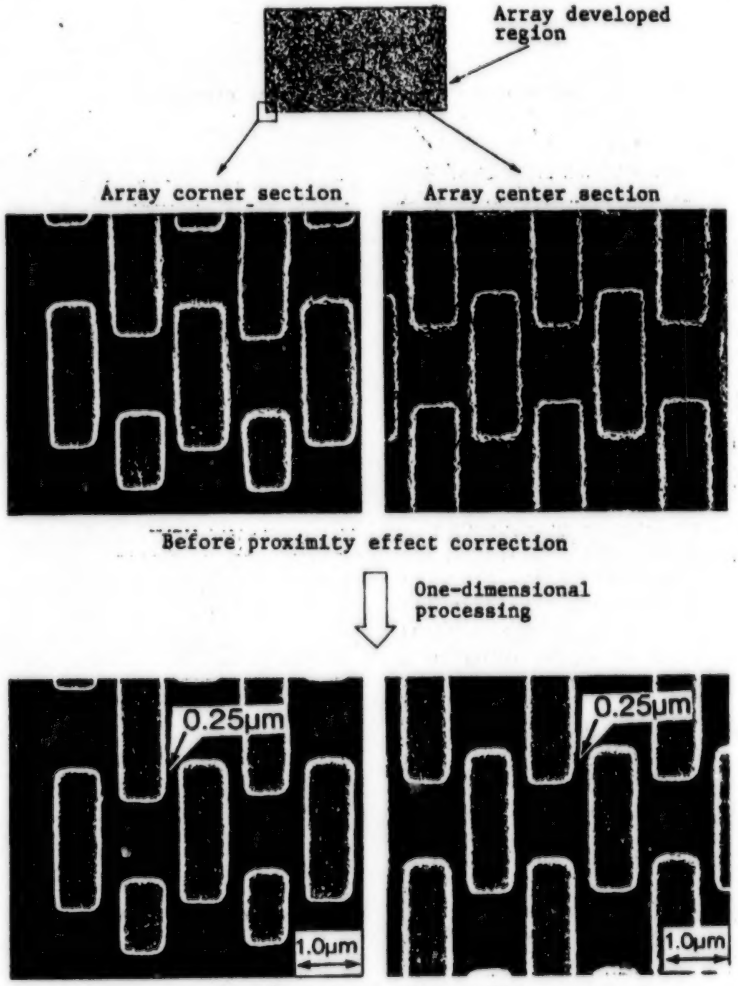

Figure 7. Before and After One-Dimensional Proximity Effect Correction

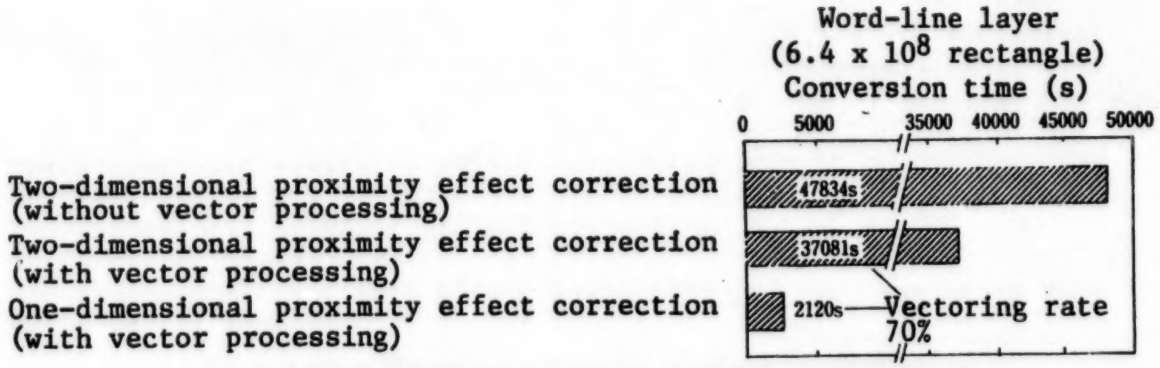

Figure 8. Result of Performance Evaluation (Application to 256M DRAM)

correcting the proximity effect) can be determined by a primary line integral calculation considering only the drawing intensity in the X-axis direction, the drawing intensity calculation time can be reduced.

By optimizing the weight of the drawing intensity, the processing at the corner sections of the array-developed region becomes possible in the same way as at the array center section and a satisfactory pattern can be obtained as shown in Figure 7.

Figure 8 shows the conversion time when the above is applied to the word-line layer. The conversion time when vector processing and one-directional proximity effect correction are applied is drastically reduced to about 1/20 of the conversion time with two-dimensional processing without vector processing. Also, as a result of applying the one-dimensional proximity effect correction to other layers of the prototyped 256M DRAM, we could reduce the conversion time to a practical period of 30 to 50 minutes, and the proximity effect would be corrected satisfactorily.

Conclusion

We applied EB direct-drawing technology using variable-shape electron-beam drawing equipment (accelerating voltage 20 kV, current density 10 A/cm^2) to the prototyping of a 256M DRAM using the 0.25 μm rule. Actual prototyping was hybrid with i-ray technology and EB direct-drawing technology used for layers with the 0.25 μm rule.

Aiming at stable operation of EB equipment and the improvement of its alignment accuracy, we analyzed the accuracy factors of the prototype, developed a technique for optimization of the correlation parameters (EB equipment technology), optimized the multi-layer resist process (partially single-layer resist process) (resist process technology) and developed the two-level data compression technology for large-capacity data and one-dimensional proximity effect correction technology (pattern data processing technology).

As a result, we were able to produce the prototype 256M DRAM shown in Figure 9 [photo not reproduced], with an alignment accuracy of no more than 0.075 μm (3 σ).

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